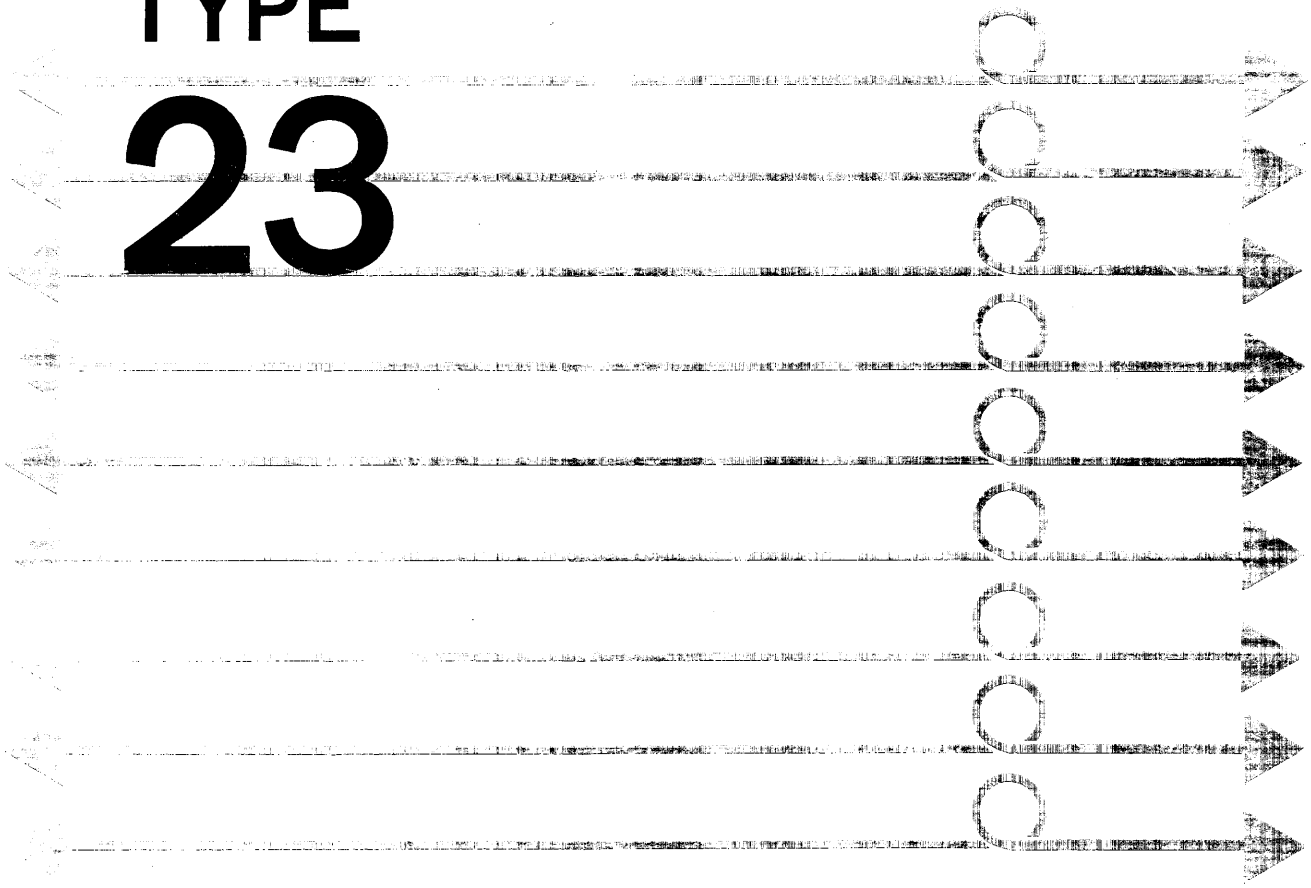
PARALLEL DRUM TYPE 23



DIGITAL EQUIPMENT CORPORATION • MAYNARD, MASSACHUSETTS

digital

PARALLEL DRUM
TYPE 23

INSTRUCTION MANUAL

COPY NO. 0164

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PREFACE

This manual contains information on the principles of operation, and procedures for installation, operation, programming, and maintenance of the Digital Equipment Corporation Type 23 Parallel Drum. The parallel drum is designed for use as a data storage device to augment the main memory of a PDP-1D computing system. Section 1 of this manual presents information of a general nature which is applicable to the entire machine. Section 2 explains the principles of operation of the parallel drum as a system and of each functional element of the system. Sections 3 through 6 present information and procedures which allow personnel to install, operate, program, and maintain the equipment. Appendixes contain information on the diagnostic program used to test the parallel drum, circuit data for modules which are unique to drum systems, and engineering drawings.

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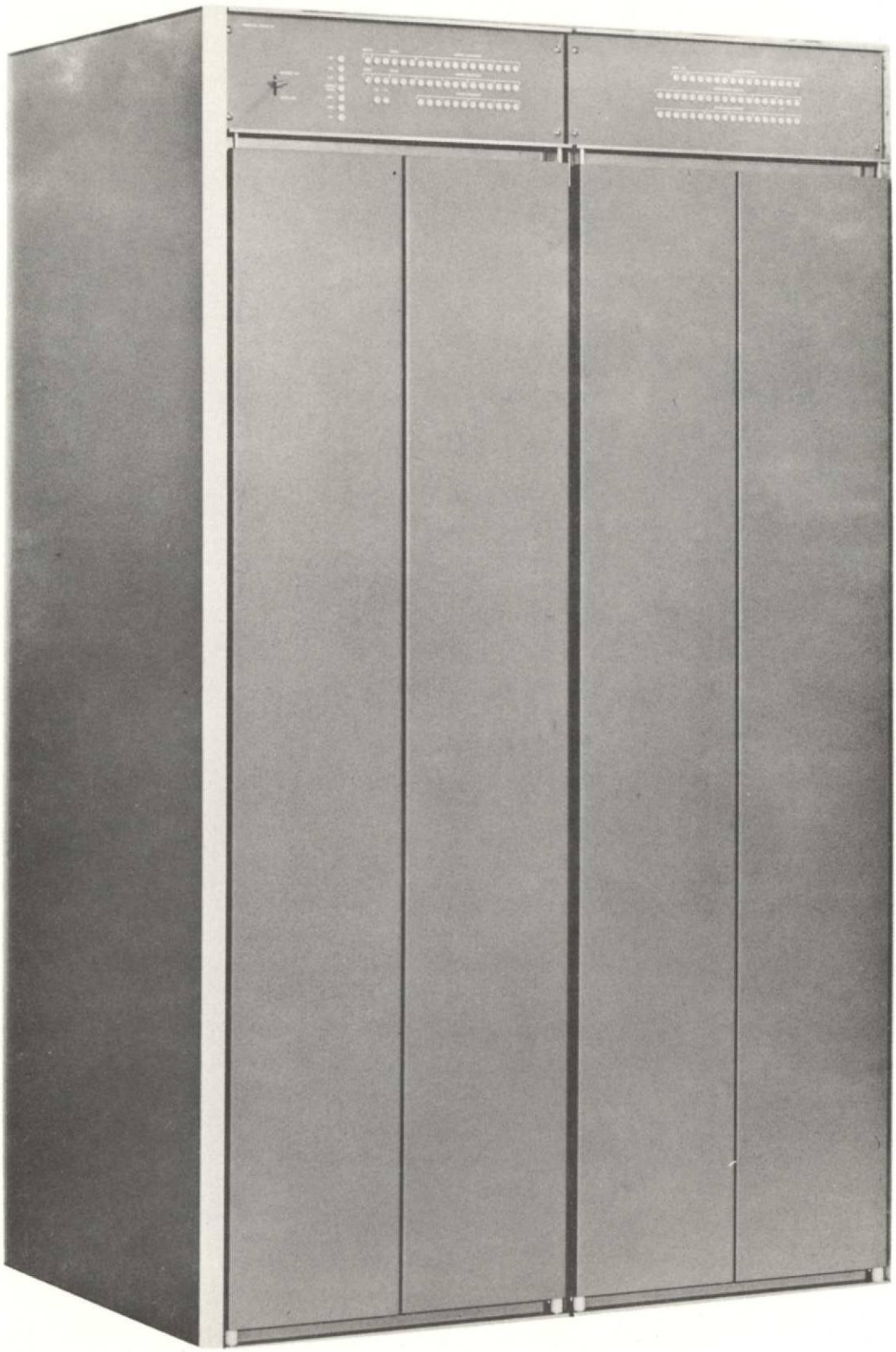


Figure 1-1 Typical Parallel Drum System Type 23

SECTION 1

INTRODUCTION

The Digital Equipment Corporation (DEC) Type 23 Parallel Drum serves as auxiliary data storage for the core memory of a Programmed Data Processor -1D and facilitates time shared use of the computer. Information in the computer can be stored (written) in the parallel drum and retrieved (read), or can be simultaneously read and written in a swap or data exchange. The drum contains 32 fields; each field is capable of storing 4096 words. Each word contains 18 information bits and an odd parity bit. The parity bit is generated within the drum during write operations and is checked during read operations to provide a means of checking the 18-bit information transfer between the drum and the computer. All transfers are completely automatic as controlled by the computer program. Transfers of from 1 to 4096 words can be executed at a rate of 8.5 microseconds per word, exclusive of set-up and access time. Transfer or exchange of 4096 words is accomplished in approximately 35 milliseconds.

FUNCTIONAL DESCRIPTION

The basic functions of the Type 23 Parallel Drum are data storage and retrieval, computer core memory address control, drum track and field selection, data request and transfer control, error checking, and power supply and distribution. Functional operation of the machine is initiated by receipt of IOT pulses from the computer. Three computer instructions produce all of the IOT pulses required to enact a transfer between the computer memory control and the parallel drum, regardless of the word length of the transfer.

A power supply and distribution network within the parallel drum produces and controls the operating voltages required by all circuits of the machine. One source of external ac power is required to energize the machine; control of this source within the machine can be exercised locally or remotely at the computer.

In response to IOT pulses from the computer the parallel drum receives the drum address from the computer, receives the number of words to be transferred and the read/write/exchange status of the transfer, and receives the core memory address of the transfer from the computer.

The transfer is then enacted in either the program interrupt or sequence break computer modes. Eighteen bits are simultaneously read from or written on the surface of the continually rotating drum and are transferred to or from the computer memory control element by means of a bi-directional pulse bus transceiver. During a write operation, a parity bit is generated within the drum for each word received from the computer so that 19-bit words are written on the drum surface. In reading data from the drum, the parity of the word is checked to assure proper transmission. Error circuits in the machine check for parity error during read cycles and check for data transmission timing during both read and write cycles. If bits are picked up or dropped out, if data received from the computer is late during a write cycle, or if data is late in being stored in the computer core memory during a read cycle, an error flag is set and a signal is sent to the computer and the transfer is halted. The computer program can interrogate the drum to determine the error status and the type of error detected when the error flag is set.

Control circuits within the parallel drum initiate the computer break status for the transfer, indicate the completion of a transfer by means of a flag, and signal the detection of an error, in addition to performing the normal internal control operations.

PHYSICAL DESCRIPTION

The parallel drum is constructed of two standard DEC computer cabinets bolted together to form a cabinet 60-1/8 inches high, 47 inches wide, and 27-1/16 inches deep. All indicators and the power control switch are located on panels at the front of the machine. Additional controls, used to inhibit writing in each of the drum fields independently and to force an incorrect parity bit as a check of the error circuits, are located on a switch panel inside the front doors of the right-hand cabinet. Eight casters allow mobility of the 900-pound machine.

Each cabinet is constructed of a welded steel frame covered with sheet steel. Double rear doors are held closed by magnetic latches. A full-width plenum door provides mounting for the Type 813 Power Control and two Type 728 Power Supplies inside the double rear doors. The plenum doors are latched by a spring-loaded pin at the top. Plug panels, which accept the signal cables from the computer, and module mounting panels are located in the front of the machine with the wiring side outward. A fan mounted in the bottom of each cabinet draws cooling air through a dust filter in the bottom, passes it over the electronic components, and exhausts it through louvered panels and openings in the cabinet.

A coordinate system is used to locate cabinets, module mounting panels, modules and signal cable connectors, and terminals within the machine. As viewed from the front, cabinet 1 is on the left and cabinet 2 is on the right. Each 5-1/4 inch position on the front of the cabinet is assigned a capital letter, beginning with A at the top. Modules are numbered from 1 through 25 from left to right in a mounting panel, as viewed from the wiring side. Connectors on a plug panel are numbered from 1 through 6, from left to right as viewed from the front of the machine. Blank module and connector locations are numbered. Terminals on a module connector are designated by capital letters from top to bottom. The letters G, I, O, and Q are omitted from module and terminal designations. Therefore, 1C06J is in cabinet one (1), the third component location from the top (C), the sixth module from the left (06), and the ninth terminal from the top of the module (J). Components mounted on the plenum door are not identified by location. Figure 1-2 indicates the location of components within the parallel drum.

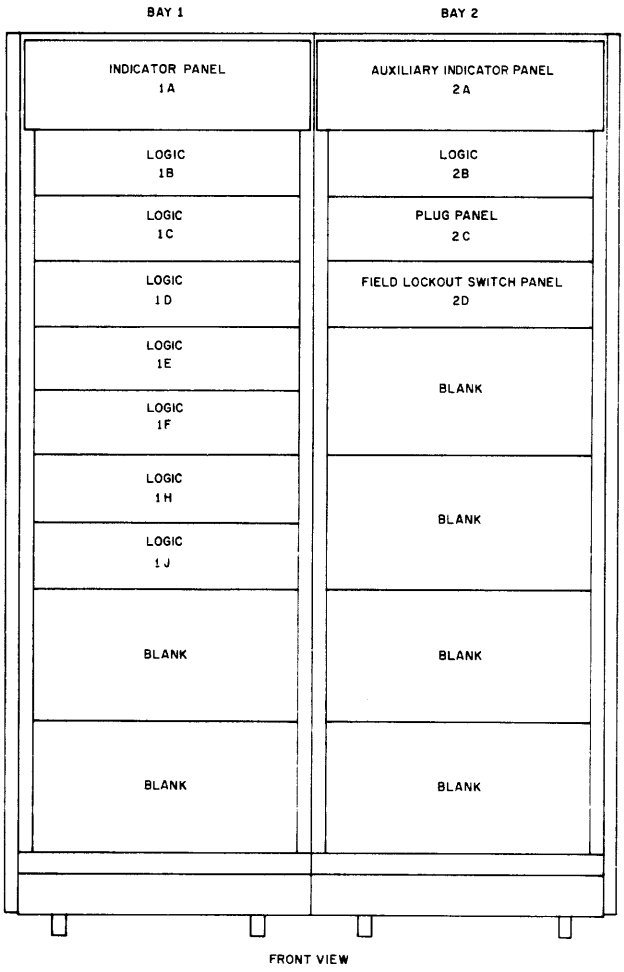


Figure 1-2 Component Locations

SPECIFICATIONS

Dimensions	47 inches wide, 27-1/16 inches deep, 69-1/8 inches high
Service Clearances	8-3/4 inches in front 14-7/8 inches in back
Weight	1000 pounds
Power Required	115 volts, 60 cycles, single phase, 10-ampere starting current, 9-amperes running current
Power Dissipation	750 watts
Power Control Point	Local or remote (computer)
Initial Starting Delay	20 minutes
Heat Dissipation	2558 BTU/Hours
Signal Cables	Three 50-wire shielded and one 18-wire coaxial
Temperature	32 to 105 degrees F operating range
Drum Motor	115 volts, single phase, 4-pole induction capacitor start and run
Magnetic Head Interference	Maximum interchannel read cross talk at least 25 db below nominal signal level. Maximum noise in any channel at least 25 db below nominal signal level.
Write Current	1.75 amperes at - 14 volts for 19 heads
Read Current	20 milliamperes at +4 volts for 19 heads
Pulse Repetition Rate	8.5 microseconds
Drum Revolution Time	35 milliseconds

SYMBOLS AND TERMINOLOGY

Engineering drawing numbers for this equipment contain five pieces of information, separated by hyphens. Read from left to right these bits of information are a 2-letter code specifying the type of drawing, a 1-letter code specifying the size of the drawing, the type number of the equipment, the manufacturing series of the equipment, and a 2-digit number specifying the number of a drawing within a particular series. The drawing type codes are:

a. BS, block schematic or logic diagram

b. CL, cable list

c. PW, power wiring

d. RS, replacement schematic

e. TFD, timing and flow diagram

f. UML, utilization module list

g. WD, wiring diagram

Symbols used on engineering drawings to represent basic logic circuits are defined in Figure 1-3.

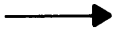
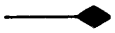
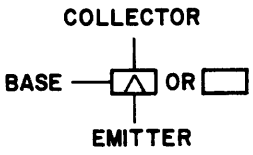
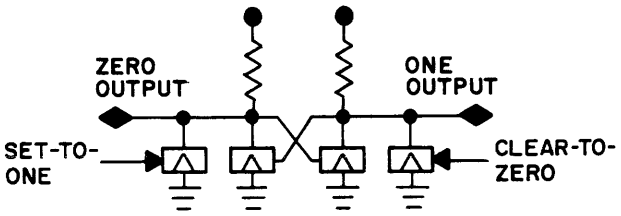
Symbol	Definition
	Standard DEC Positive Pulse or positive-going transition
	Standard DEC Negative Pulse or negative-going transition
	Standard DEC Ground Level signal
	Standard DEC Negative Level (- 3 vdc signal)
	Load resistor clamped at - 3 vdc
	Transistor inverter
	Bistable multivibrator (flip-flop constructed of two cross-coupled inverters.

Figure 1-3 Logic Symbols

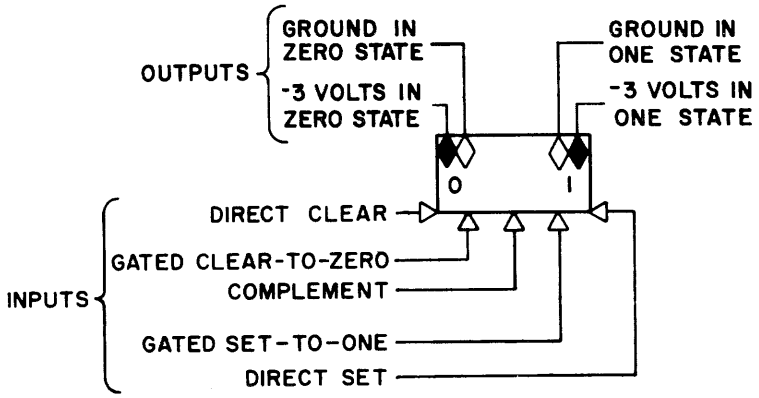
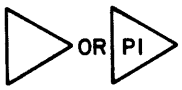
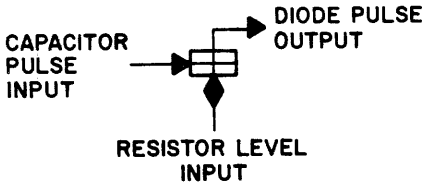
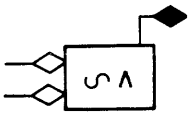
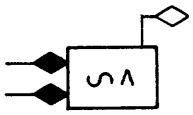
Symbol	Definition
	Flip-flop constructed of fixed connections within a systems module.
	Pulse inverter
	Capacitor-diode gate (negative or positive as indicated by signal inputs).
	Inverting diode gate used as an AND circuit for ground-level signals.
	Inverting diode gate used as an AND circuit for negative-level signals.

Figure 1-3 Logic Symbols (continued)

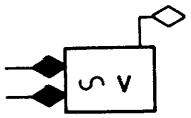
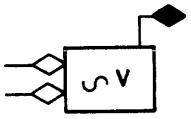
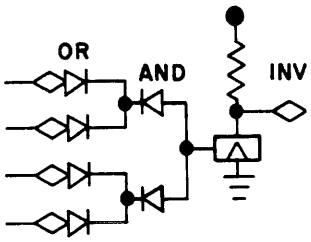
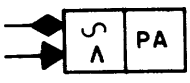
Symbol	Definition
	Inverting diode gate used as an OR circuit for negative-level signals.
	Inverting diode gate used as an OR circuit for ground-level signals.
	Diode OR and AND circuit followed by inverter.
	Inverting diode gate used to trigger a pulse amplifier.

Figure 1-3 Logic Symbols (continued)

Abbreviations and conversions used in this manual, on the engineering drawings, or on panel markings are defined in the following list.

Circuit Blocks

ACT	Active flip-flop
DBA SYNC	Drum break address flip-flop
DC	Drum counter
DCL	Drum core location
DRA SYNC	Drum read address flip-flop
ERROR SYNC	Error synchronization flip-flop
IL	Initial location
PA	Pulse amplifier circuit
PE	Parity error flip-flop
PI	Pulse inverter circuit
RFB	Read field buffer
RQ	Request flip-flop
SA	Sense amplifier (reader)
TRA	Transfer status flip-flop
TRANS ERROR	Transfer error flip-flop
WC	Word counter
WFB	Write field buffer

Signals

ACT	Active flip-flop or level
ADRS ACK	Address acknowledge pulse
DBA	Drum break address instruction or flip-flop
DC=IL	Level indicating C(DC) = C(IL)
DC => IO STROBE	Pulse which strobes C(DC) => C(IO)
DCL	Drum core location instruction or register
DCT CLEAR	Drum control clear pulse
DCT DISABLE	Drum control disable level

Signals (continued)

DIA	Drum initial address instruction
DRA	Drum request address instruction or flip-flop
DWC	Drum word counter instruction
IB	In buffer register or level
IO	Input-output register or level
IOB ADRS ACK	Input-output buffered address acknowledge pulse
MA	Memory address register or levels from the DCL to this register
OB	Out buffer register or levels
PBT	Pulsed bus transceiver
PWR CLR	Power clear pulse
MB	Memory buffer register or input-output levels of the PBT
RD RS	Read restart pulse
RD REQ or RD RQ	Read request level
RFBH	Read field buffer high digit level
RFBL	Read field buffer low digit level
RQ	Request level
RQB	Request level buffered
SA	Sense amplifier circuit (reader) or pulses
SBS RETURN	Sequence break signal return pulse
TE or TR ER	Transfer error level
TP	Timing pulse
WC	Word counter register or level
WFBH	Write field buffer high digit level
WFBL	Write field buffer low digit level
WFD	Write field disable buffer
WFLO	Write field lockout switch or level
WR REQ or WR RQ	Write request level
WR WS	Write restart pulse

Subscripts

0 through 6	Individual bit numbers of a register, counter, or flip-flops

Superscripts

1	Signal condition for flip-flop binary 1 status
0	Signal condition for flip-flop binary 0 status

Other Notations

V	Inclusive OR
$\not\vee$	Exclusive OR
$\wedge$	AND
C(A)	Contents of register A
A => B	A replaces B or B is set to A
$C(A)_{0-5} => C(B)_{6-11}$	The contents of bits 6 through 11 of register B are set to correspond with the contents of bits 0 through 5 of register A.

PERTINENT DOCUMENTS

Publications

The following DEC documents serve as source material and complement the information in this manual:

a. Digital Modules Catalog, A-705. This book presents information pertaining to the function and specifications for the basic systems modules and accessories comprising the Type 23 Parallel Drum.

b. Silicon Modules Catalog C-6000. Information on the function and specifications for the 6000 series system modules is contained in this book.

c. PDP-1 Handbook, F-15. Programming information for the Programmed Data Processor-1 is presented in this document.

d. PDP-1 Supplements, F-15(1D-45) and F-15 (1D-48). These documents describe the special instructions added to the PDP-1 when used in a typical PDP-1D configuration, such as that at Bolt Beranek and Newman, Inc.(45) and at Stanford University (48).

e. PDP-1 Maintenance Manual, F-17. Installation, operation, and maintenance of the standard PDP-1 and its central processor options are covered in this manual.

f. Parallel Drum Diagnostic Program Tape, DEC-1-137-M. A perforated- paper tape and program resume of a routine which tests the data reading, writing, and swapping operations of the drum system.

Engineering Drawings

Engineering drawings in the following list are reproduced in Appendix 3 of this manual as an aid to understanding and maintaining the Type 23 Parallel Drum. A complete set of formal engineering drawings is supplied separately with each system. Should any discrepancy exist between the drawings in this manual and those supplied with the equipment, assume the formal drawings to be correct.

Power Supply and Control

Power Supply RS-728
Power Control RS-813
AC-DC Wiring PW-D-23-0-8

System Modules

Clamped Load Resistors RS-1000
Three-Bit Parity Circuit RS-1130
Delay (monostable multivibrator) RS-1304
Delay Line RS-1310
Pulse Generator RS-1410
Drum Sense Amplifier (reader) RS-1537

System Modules (continued)

Logic and Wiring

SECTION 2

PRINCIPLES OF OPERATION

RECORDING AND PLAYBACK TECHNIQUE

The Type 23 Parallel Drum utilizes return-to-bias recording techniques which lend themselves to the simultaneous read and write, or exchange, operation required of the drum. In each bit cell the new information to be written in a field is available just before the information is to be read from another field. Because of noise considerations, the read strobe must precede the write strobe. The effective advance of the read strobe over the write strobe, which previously wrote the information to be read, is possible because of the fringing of flux ahead of the data head gap. Before a transfer begins the read and write head select circuits are enabled. At the beginning of a transfer bias current is applied to the write-selected heads so that all transients occur and damp out before the occurrence of the read strobe. In a data exchange operation the read strobe is followed by the write strobe, and write noise is induced in the sense amplifier. This noise is commonly of greater amplitude than the read signal; however, this noise damps out before the next read strobe occurs. The read and write current waveforms and the timing of the read strobe and write strobe are indicated in Figure 2-1.

BLOCK DIAGRAM DISCUSSION

Functional elements of the parallel drum are shown on engineering drawing BD-D-23-0-17. This drawing indicates all signals which flow between the elements of the drum, and between drum elements and the PDP-1D and the Memory Control. The only signals which are not indicated are the phase signals out of the timing element which go to all logical blocks and the operating voltages which also are supplied to all elements from the power supply and distribution element. Detailed information on each of the functional blocks is indicated in block schematic engineering drawings BS-D-23-0-2 through 6, and complete information transfer flow in timing operations is indicated in engineering drawing TFD-D-23-0-1. The distribution and wiring of the power circuits within the parallel drum are indicated in engineering drawing PW-D-23-0-8. As reference is made to these drawings in the following text, only the final portion of the engineering drawing number will be used. Reference will also be made by means of the coordinates

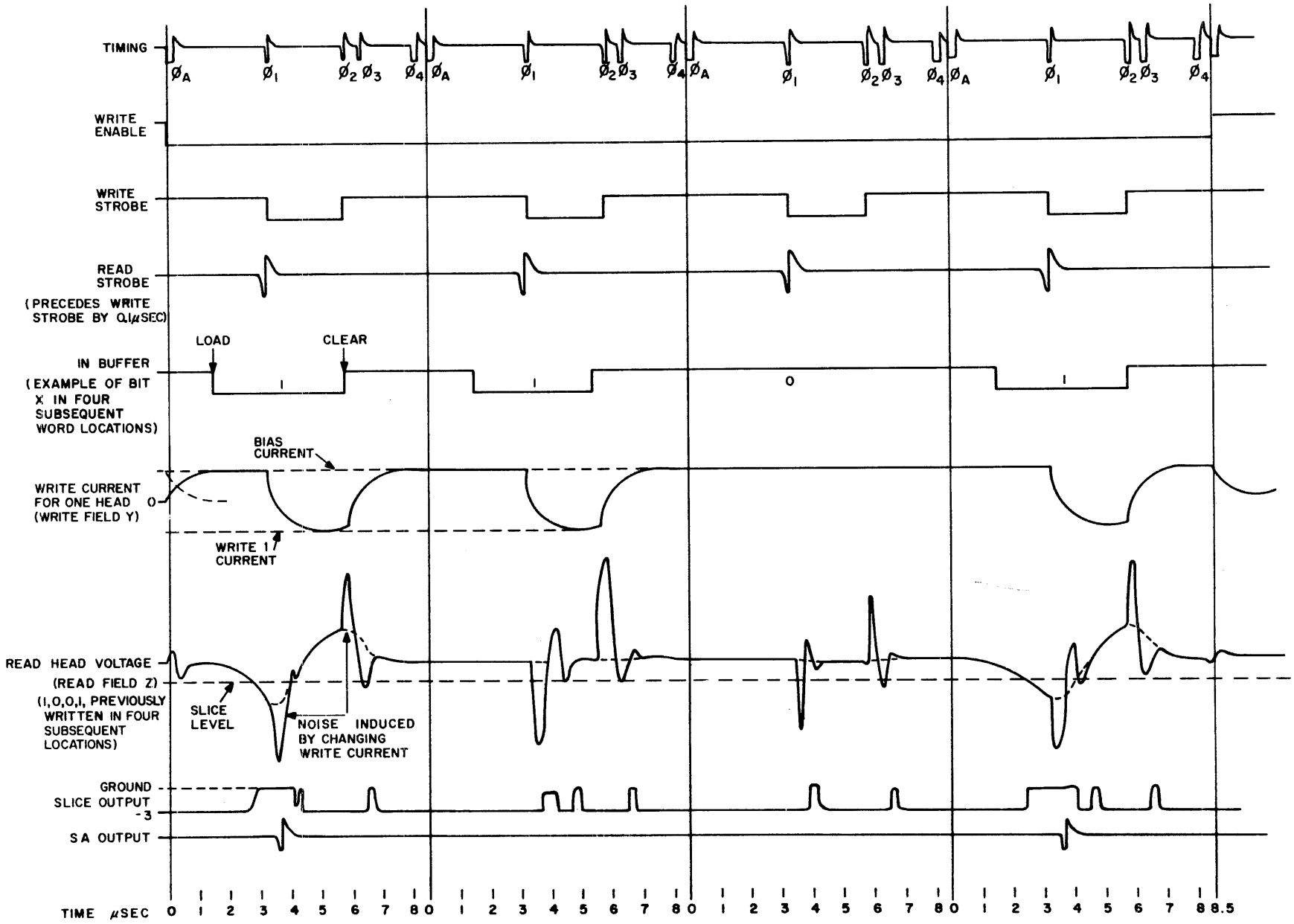


Figure 2-1 Typical Recording and Playback Timing

on the drawing. These coordinates are A through D from top to bottom and 1 through 8 from left to right; so zone A1 is in the upper left hand corner, and zone D8 is in the lower right hand corner. Note that register bits are numbered to correspond with the computer register bits to which they transfer data. Therefore, most register bits are numbered so that the least significant bit is designated bit 17.

Index and Clock Readers

In addition to the normal data tracks recorded on the drum surface, two tracks provide timing information used in the control of normal drum operations. These two tracks are the index and the clock tracks. The information on these tracks is prerecorded and is read from the index track by the Type 1537 Drum Sense Amplifier module at location 2B6 and is read from the clock track by the Type 1537 module at location 2B5. One index bit is recorded on the surface of the drum to indicate the starting address of all words written on the data tracks. The output signal level from the index sense amplifier initiates operation of a Type 1304 Delay module whose negative pulse output clears the drum counter and signifies the start of each new drum cycle. The delay is provided to allow adjustment of the timing relationship of an index pulse so that it occurs exactly in the center of the time between the first and last clock pulse. The output of the clock sense amplifier initiates operation of a Type 1410 Pulse Generator module at location 2B4 to produce a standard DEC 70-nanosecond clock pulse which initiates operation of the timing element and controls the timing of all operations in the parallel drum. There are 4096 clock bits recorded around the surface of the drum; each clock pulse signifies a data bit cell location. Engineering drawing 4 contains this logic in the lower left hand corner.

Timing

The timing element consists of a timing chain generator composed of delay lines, delays, and pulse amplifiers which produce the read strobe, write strobe, phase 1, phase 2, phase 3, phase 4, and phase A pulses. The timing chain is initiated by receipt of a clock pulse from the clock reader element. Transistor gating circuits allow generation of the read strobe signal only when the drum is in the read mode and in the active status. The phase 1 signal can be generated only when the drum is in the write mode and in the active status. The phase 2 and phase 3

signals are enabled only when the drum is in the active status. The phase 4 and phase A pulses cannot be disabled. In addition to these pulses the timing element produces the DCT disable signal, which is a constant - 3 vdc level produced by clamped load resistors. This level is used wherever constant enabling or disabling - 3 vdc levels are required. The phase 3 signal initiates operation of the Type 4604 Pulse Amplifier in location 1F4 whose output is the write restart (WR RS) signal, which is supplied to the memory control and to the parity formation element.

Control

The control element contains nine flip-flops (TRA, RQ, ACT, ERROR SYNC, TRANS ERROR, PE, DRA SYNC, DBA SYNC, and busy) which determine and control the status of the parallel drum. This element is shown on engineering drawing 2, above the timing element and the parity check element. When power is initially applied to the parallel drum, the Type 4401 Clock at location 1F2 is enabled by a ground level supplied to terminal B and produces repeated power clear pulses. The power clear pulses clear the parity formation element and various registers of parallel drum in addition to all of the flip-flops in the control element. After an initial delay period of approximately 30 seconds, the normally closed contacts of time-delay relay D2 of the Type 813 Power Control open to remove the ground potential from the integrating circuit at the input of the clock module to disable it.

The nine control flip-flops are also cleared by receipt of the DIA 7-4 command pulse, which is received during the first instruction in the initializing sequence. All of the flip-flops except the busy flip-flop are set to one or cleared to zero by the phase A pulse, as a function of the condition of level signals supplied to capacitor-diode gates. The busy flip-flop is constructed of two cross-coupled inverters which function as an unbuffered flip-flop. This flip-flop is cleared to zero by power clear pulses, the DIA 7-4 pulse, or a sequence break signal return and is set to 1 by the DCL 10-4 pulse. The function of the other flip-flops can be determined by the control signal or IOT pulse inputs required to set or clear them.

Drum Counter (DC)

The DC is a 12-bit counter which keeps track of the angular position of the continually rotating drum. This register is cleared by the index pulse provided by the index reader, and is incremented

by one by each phase A pulse. Both the 1 and 0 outputs from each bit of this register are supplied to a comparator so that a data transfer is requested when the drum reaches the position, or drum address, set into the initial location register. The contents of this register can also be set (read) into the PDP-1D IO register to monitor the angular position of the drum. The logic circuits for the DC are shown on zone B of engineering drawing 6.

Initial Location Register (IL)

The IL is a simple set-and-reset 12-bit register which is used to store the initial address or first address at which the drum is to read or write. During either a DIA or DBA instruction, the register is cleared at computer 7 time and is set to the address contained in IO bits 6 through 17 at computer 10 time. Both the 1 and 0 outputs from this register are continually supplied to a comparator for comparison with the contents of the DC. This register is shown on zone C of engineering drawing 6.

Comparator

The comparator, shown on zone B8 and C8 of engineering drawing 6, continually monitors the contents of the DC and the IL. The circuit provides a bit-by-bit exclusive OR comparison of the contents of these two registers and supplies the negative DC = IL signal to the control circuit when the two registers contain the same drum address. This signal causes the control circuit to set the request flip-flop to the 1 status if the transfer flip-flop is also in the 1 status. The output of this flip-flop is then supplied to memory control to request a transfer. When using the DBA instruction, the DC = IL signal also initiates generation of the sequence break signal return pulse which is supplied to the computer to initiate a transfer through the sequence break mode, and clears the busy flip-flop.

Word Counter (WC)

The WC is a 12-bit binary counter which controls the number of words transferred during any drum operation. The WC logic is shown on zone A of engineering drawing 6. During a DWC instruction, the contents of the computer IO register are set into the write control, the write field buffer, and the word counter. At this time the IO register information contained in bits 0 through 5 determines if writing is to occur in the following transfer and the write field to

be enabled. The contents of bits 6 through 17 of the IO register specify the number of words to be transferred. The 1's complement of the contents of bits 6 through 17 of the computer IO register is set into the contents of the word counter at computer time 10 (the WC is cleared at computer 7 time by the DWC instruction). During the ensuing DCL instruction, the contents of the WC are incremented by one by the DCL 7-4 IOT pulse; therefore when the transfer is initiated by the DCL instruction, the word counter holds the 2's complement of the number of words to be transferred. As each word is transferred, the write strobe pulse increments the contents of the WC. The write strobe pulse is used for this operation since both reading and writing have been completed at the current drum address when this pulse occurs. Therefore, when the specified number of words have been transferred, the most significant bit of the WC changes from the 1 state to the 0 state. The WC_6^0 signal clears the request flip-flop in the control element to signify to the computer that the transfer is complete.

Drum Core Location Counter (DCL)

The DCL is a 16-bit register which specifies the computer core memory address to or from which the next word is to be transferred. The contents of the DCL are sampled by the memory control and set into the contents of the core memory address register for each word of a transfer. Bits 6 through 17 of the DCL function as a setable counter which is automatically incremented by receipt of the IOB address acknowledge pulse from memory control. Bits 2 through 5 of the DCL are always transferred into the memory address register as they are set by computer IO register bits during the DCL instruction program initialization. Bits 2 and 3 specify one of four 16,384-word memory banks to be used for the transfer, and bits 4 and 5 specify one of four 4096-word memory modules within the memory bank. Therefore, the parallel drum is capable of operating with a computer containing 65,536 words of core memory with a maximum transfer word length of 4096 words. The DCL is shown on zones C and D of engineering drawing 6.

Before normal drum transfer operations, the DCL is cleared by the power clear pulses. During the third IOT instruction of the drum initialization program, the DCL instruction clears the DCL at computer 7 time and sets the contents of the IO register into the contents of the DCL at computer 10 time. Bits 6 through 17 of the DCL are incremented at the completion of each word transfer by the IOB address acknowledge pulse. All outputs from the DCL to the memory control are buffered by a non-inverting Type 1684 Bus Driver module.

Read Control and Read Field Buffer (RFB)

Read control is a single flip-flop which determines if reading from the drum is enabled or disabled during any data transfer. The flip-flop is set to the 1 status (to enable reading) or to the 0 status (to disable reading) by the contents of IO register bit 0 during the first instruction of the drum initialization program (DIA or DBA instruction). The 0 output from the read flip-flop is buffered by circuit HJ on the Type 6102 Inverter module at location 1F22 to produce the read buffered (B) signal. This buffered signal, supplied to the timing element and to the control element, is a - 3 vdc level when the flip-flop is in the 0 status and is a ground level signal when the flip-flop is in the 1 status. When the read flip-flop is in the 1 status, transistor gating circuits in the timing element are enabled to produce the read strobe pulse, thereby allowing read operations to take place. When the read flip-flop is in the 1 status, the read buffer signal supplies one input to the UVW circuit of the Type 6113 Diode Unit module at location 1E15 whose output is buffered by the Type 1684 Bus Driver at location 1F3 to provide both the read request (RD RQ) and write request (WR REQ) signals supplied to the memory control.

The 5-bit RFB specifies one of the 32 read fields which is to be activated during the ensuing transfer. The contents of the RFB designate a drum read field address of the transfer and are specified as a 2-digit octal number. Bits 1 and 2 of the RFB output are decoded to form the most significant bit of the octal number or the read field buffer high (RFBH) portion of the octal number which may run from 0 through 3. Bits 3 through 5 of the RFB are decoded to form the least significant bit or read field buffer lower (RFBL) portion of the octal drum address which may run from 0 through 7.

Both the read control flip-flop and the RFB are cleared by the DCT clear pulse, which is produced by the control element when the drum receives a DIA 7-4 command pulse. Both the read control flip-flop and the RFB are set to correspond with the contents of computer IO register bits 0 through 5 upon receipt of either a DIA 10-4 or DBA 10-4 command pulse from the computer. Note that the circuit contains inverters KL and UV on the module in location 1F8 which provide the required inversion for operation of the negative capacitor-diode gates at the input to the read control and RFB_1 flip-flops. The read control and RFB are shown on the lower right hand portion of engineering drawing 5.

Write Control and Write Field Buffer (WFB)

The write control and WFB determine the write status of the drum and control the drum write field address. Both the write control and WFB flip-flops are cleared by the DCT clear pulse, which is produced when the control element receives a DIA 7-4 command pulse. Both the write control and WFB are set to correspond to the contents of the computer IO register bits 0 through 5 by the receipt of a DWC 10-4 command pulse from the computer. As in the read control and RFB, the output from the write control flip-flop is supplied to the control element to produce the read request and write request signals, and the five bits of the WFB are divided to produce a 2-digit octal number varying from 0 through 37. The 0 output of the write control flip-flop is buffered by two parallel-connected bus drivers in the module at location 1E3. This buffered output is supplied to each gate in the drum field select element to assure that writing does not occur when the write control flip-flop is in the 0 status. This logic is shown on the lower left hand corner of engineering drawing 5.

Drum Field Select

Selection of the drum field, or address, of a transfer is performed by decoding and gating circuits shown in zones A, B, and C of engineering drawing 5. The decoding involves negative AND gates which combine the appropriate outputs of the most significant bits of the WFB and RFB to produce the WFBH 0 through 3 signals and the RFBH 0 through 3 signals. Normal binary-to-octal decoders are used to combine the outputs of the four least significant bits of the WFB and RFB to produce the eight WFBL and RFBL signals (Type 4151 modules at location 1E16 and 1E21, respectively). Each of the 32 field select lines supplied to the data head selection diode matrix within the drum housing is connected to the output of two negative AND diode gates within a Type 4519 Drum Field Select module. Therefore, each line is selected by diode gating which combines the appropriate RFBH and RFBL information or which combines the appropriate WFBH and WFBL information with the condition that the write control flip-flop is in the 1 status and the appropriate WRITE FIELD LOCKOUT (WFLO) switch is in the down or enable position. The WRITE FIELD LOCKOUT switches are located on panel 2D at the front of the parallel drum and are used to inhibit writing in fields containing data which is not to be destroyed. Placing any of these octally numbered switches in the up position supplies the DCT disable - 3 vdc level signal to terminal R of the appropriate drum field select module, thus inhibiting writing. With

the switches in the down position a ground level is supplied to terminal R and the gating is enabled.

Pulsed Bus Transceiver

The pulsed bus transceiver provides a means of transmitting bidirectional data between the parallel drum and the memory control. The transceiver is a quadruple size standard DEC Type 1665 module located in positions 1H24 and 1J24. This module consists of two sets of 18 2-input negative AND diode gates and 18 output pulse amplifiers. Each of the pulse amplifiers is triggered by one of the diode gates. The 18 input diode gates all receive one input from a different bidirectional signal line which is connected by a coaxial cable to a similar pulsed bus transceiver within the memory control. The second input to each of the input diode gates is common to allow sampling of the information of the signal lines when the address acknowledge pulse is received from the memory control. The output from these diode gates provides a direct set input to the in buffer. Each of the 18 output diode gates receives an input from the output of one bit of the out buffer. The second input to each of the output diode gates is common and is connected to a pulse amplifier output which is triggered by the phase 3 pulse. The output from each of these diode gates triggers a pulse amplifier, causing it to pulse a bidirectional signal line. Therefore, when the phase 3 pulse occurs, the contents of the out buffer bits containing a 1 cause a negative pulse to be applied to the appropriate bidirectional signal line of the pulsed bus transceiver. Coaxial cables connect the pulsed bus transceiver in the parallel drum to a pulsed bus transceiver within the memory control, providing an efficient link of memory buffer register information between the two units. The pulsed bus transceiver module and the two pulse amplifier modules which functionally operate as the pulsed bus transceiver are shown in zones A and B of engineering drawing 3.

In Buffer (IB)

Data to be written on the drum is received in parallel from the 18 bits of the pulsed bus transceiver. The in buffer stores this information temporarily and supplies it to the data writers and to the parity formation circuit. When parity is formed, the write parity bit is also supplied to the data writer so that 19-bit words are written. The in buffer also functions in exactly the same manner during data reading so that the 19 information bits read by the data reader are

transferred to the out buffer, then are transferred from the out buffer to the pulse bus transceiver and then are transferred to the in buffer. The in buffer supplies the 18 bits of the word just read to the parity formation circuit, and a new write parity bit is formed. This bit is compared with the parity bit just read by the data reader and causes an error signal to be produced in the control element if the parity bit read in the new write parity bit formed is not identical.

Engineering drawing 3 shows the in buffer in zone A to consist of 18 flip-flops, each composed of two cross-coupled transistor inverters. Each flip-flop is set to the 1 status by a positive pulse from the output of the associated input diode gate in the pulsed bus transceiver, and is cleared by an inverted negative pulse produced at phase 2 time or when the address acknowledge pulse is received.

Out Buffer (OB)

The out buffer provides temporary storage of data, which has been read by the data readers, until the information can be sent to the memory control via the pulsed bus transceiver. Since the memory control uses a split memory cycle, information read from core memory is not rewritten automatically. Data transfer from memory control to the in buffer during a write only operation is transferred to the data writer and to the out buffer. The data can then be restored in core memory from the out buffer. This operation takes place as follows. At phase 1 time instead of strobing new information from the data readers into the out buffer, the word which was read from the memory control exists in the in buffer and is transferred to the out buffer. Writing takes place in the normal fashion, and at the end of the write strobe the in buffer is cleared. Then at phase 3 time the word in the out buffer is returned to memory control to restore the word which was previously read from computer core memory and written into the in buffer.

The out buffer is composed of 18 unbuffered flip-flops constructed of two cross-coupled transistor inverters and appropriate gating for set and clear inputs. This logic is shown on zone C of engineering drawing 3. Each bit of the out buffer is cleared by the inverted negative pulse produced by the IOB address acknowledge pulse. During a read operation, the data reader information (designated SA_0 through SA_{17}) is a negative pulse to signify a binary 1. The positive pulses produced by inverting SA_0 through SA_{17} provide a direct set for the appropriate

bit of each out buffer flip-flop. During a write only operation, the contents of the in buffer are supplied to the level input of a Type 4127 Capacitor-Diode-Inverter module, which is triggered at phase 1 time to produce the positive pulse required to set the appropriate bit of the out buffer.

Parity Formation

The parity formation circuit continually generates the write parity signal according to the contents of the in buffer and supplies this signal to the control element and to the write parity bit of the data writer (for bit P). The write parity signal is generated by combining the outputs of eight Type 1130 Three-Bit Parity Circuit modules, each of which provides a parity check of three input bits. The first six Type 1130 modules compare the contents of three bits of the in buffer. The output from three Type 1130 modules is compared again in another Type 1130 module, and the output of the last two Type 1130 modules is combined in negative AND gates formed by three of the circuits on the Type 6113 Diode Unit at location 1C3. The write parity signal is at - 3 vdc if the in buffer contains an even number of ones or is at ground potential if the in buffer contains an odd number of ones. The status of the write parity signal is compared with the status of the write bad parity flip-flop to determine the status of the write parity bit supplied to the data writer P. The write bad parity flip-flop is composed of two cross-coupled transistor inverters, which are cleared by receipt of power clear pulses or by the write restart signal, and is set to the 1 status by pressing the WRITE BAD PARITY pushbutton on the write field lockout switch panel before the transfer commences. When this pushbutton is pressed, the flip-flop is set to 1, pin V of the negative AND gate at location 1E8 becomes a ground level, and pin K of the - AND gated location 1F7 becomes a - 3 vdc level. This gating inverts the signal supplied to the drum writer. After the first word has been transferred, the write restart pulse is received from the memory control to clear the write bad parity flip-flop and restore the normal conditions for generating the odd parity bit. The WRITE BAD PARITY pushbutton is a maintenance device which allows diagnostic programs to be written with an incorrect parity bit in the first word transferred; so a diagnostic program can check the operation of the parity error circuits of the drum, or a programmer can use this switch to test the error check routines within a given program. This switch is not used in normal data transfers.

Parity Check

The parity check element compares the contents of the parity bit read from the drum with the status of the write parity signal and generates a parity error set signal if an error is detected when the drum is active and in the read status. This signal is a standard DEC positive pulse which sets the parity error (PE) flip-flop in the control element. The logic which performs this operation is shown in the lower right hand corner of engineering drawing 2.

When bit P of the data reader detects a 1, the SA_P signal is a negative pulse which is supplied to the set-to-one gate of the read parity flip-flop. This flip-flop is cleared by receipt of the read restart signal from the memory control. The status of the read parity flip-flop is then compared with the write parity signal by the Type 6113 Diode Unit at location 1E15 and 1E8. The output at terminal H of module 1E8 becomes a ground level to indicate an error condition if the write parity signal is even, and if a 0 is read from the parity bit. The output from the module at location 1E15 is negative to indicate an error if the write parity signal is odd and the parity data reader detected a 1. This ground level error signal supplies one input to a 3-inverter ground-level AND gate. The output from this AND gate is a - 3 vdc error signal only when an error is detected, when the drum is in the active state, and the read control is active. This error signal is gated again by the negative AND gate which produces the positive parity error set signal when the output of the transistor AND gate is negative at phase 4 time.

Data Writers

The 18 bits of data to be written are stored in the in buffer. The binary 1 output from each flip-flop of the in buffer is supplied to a 2-input negative AND diode gate. The second input to each of these AND gates is provided in common by the write strobe - write active signal. This signal is generated by negative AND gates and is negative for the 2.6 microsecond duration of the write strobe pulse when the drum is in the active status and in the write mode. The output from each of the 2-input negative AND gates supplies the input to one side of one bit of a Type 4518 Drum NRZ Writer module. The inverted output of the 2-input negative AND gate supplies the input to the second half of each bit of a Type 4518 module. Each half of each writer module is enabled by the write enable signal, which is a ground level signal produced by the drum being in the active state and in the write mode. The complementary outputs from each writer are supplied, through the data-head selection diode matrix, to opposite sides

of the read/write heads, through half of the head winding to the center tap. This logic is shown in zone A of engineering drawing 4.

Data Readers

Data read from the drum surface by the read/write heads is supplied, through the data-head selection diode matrix, to the input terminals of the 19 data readers, or Type 1537 Drum Sense Amplifier modules. If the data read is in the 1 status at read strobe time, the sense amplifiers provide a Standard DEC negative Pulse which sets the 18 data bits into the contents of the out buffer and sets the parity bit into the contents of the read parity flip-flop of the parity check circuit. This logic is shown on zone C of engineering drawing 4.

Data Head Selection and Drum Memory

The drum housing mounted within cabinet 2 of the Type 23 Parallel Drum contains the data-head selection diode matrix, the read/write heads mounted on a shroud, and the rotating drum memory on which data is recorded. Panels attached to each side of the drum housing by means of captive screws are easily removed to allow access without disassembly or disconnection of power and signal connections. Thus, drum maintenance can be undertaken under system operating conditions. The drum housing is designed so that the fan action of the drum circulates air around the drum and head mounts, keeping the temperature differential within the housing to a minimum. Due to aerodynamic head suspension, thermal expansion is inconsequential; therefore, this internal circulation, together with the external discharge from the fan motor, also tends to maintain a minimum differential temperature from inside to outside, so that repeated stops and starts can be made without danger of head contact. The motor, which turns the drum, is of special design to provide the fastest starting time compatable with minimum power input and power losses at nearly synchronous speed. The fan for this single-phase, four-pole, induction, capacitor-start and run motor is fastened to the bottom of the spindle. Ambient air is drawn through a shroud and over the finned motor housing. This air current takes heat away from the motor, preventing localized temperature rise.

The rotating drum assembly is designed with minimum cross-section for proper heat transfer and dissipation. It is mounted on separable inner-ring angular-contact bearings, which are prelubricated for life. Preloading is accomplished by springs at the top end of the unit. The magnetic

coating on the surface of the drum is Grimaco 6037 - X high-density dispersion, heat-cured and lapped to its final finish. Dynamic runout is less than 0.0001 inch total indicated reading.

All data, index, and clock heads are mounted in pads of eight. The pads are suspended from the shroud surrounding the drum rotor, by flexible metal reeds. When the drum rotor reaches approximately 90 per cent of synchronous speed, a 60-cycle current is applied to a heater surrounding a bimetal strip, which in turn forces the head pad toward the drum surface. Total travel of the bimetal strip is limited by a stop screw. The final running clearance between head pole piece gap and the drum surface is set by the action of the precision flat ground head pad aerodynamically flying on the liminal air film which surrounds the drum surface when at nominal speed. Initial factory adjustments are made by two differential screws which torque the reed mounting to ensure that the pad is parallel to the drum surface and tangent at the pole piece gap.

A printed-wiring board contains a 32-diode matrix used to select the eight heads on an associated pad. The connection of these diodes to a read/write head and connection to the logic elements of the drum system is indicated in Figure 2-2. This figure indicates the equivalent circuit of the logic elements as seen by the diode matrix, and indicates the flow of current using an example where field select 0 is in the read state, field select 1 is in the write state, and the balance of the field select circuits are deselected. When reading, a Type 4519 Field Select module supplies 20 milliamperes to the common field select line connected to all head centertaps for the appropriate field. A 1 milliampere current enters the centertap of each head and divides, 1/2 milliampere going through each of the forward biased diodes to the input of Type 1537 Drum Sense Amplifier (reader). The division of current is assured by the 1K equivalent resistance at each input terminal of the sense amplifier. This rise of 1/2 milliampere causes a 1/2 volt rise across each 1K resistor and places the common field select line at a read potential of +4 volts. When a field select circuit is in a write state, the centertap of the 19 common heads is returned via the field select to - 14 volts. When a field selector is in the write state, - 14.0 volts are applied to the center tap of the associated heads in the field. Since no current limiting exists, a short circuit between any potential more positive than -14.0 volts and either an outside head winding terminal or a write bus selected in this manner destroys (open)the head winding and/or the selection diodes. When the Type 4518 Drum NRZ Writers are gated on, each head returns approximately 90 milliamperes to this bus, for a total current

of approximately 1.75 amperes. A head in the read select status is isolated from the write bus by diodes which are back biased by a voltage of from 5 to 19 volts. A head which is in the write select state is disconnected from the read bus by diodes which are back biased by a voltage of from 5 to 19 volts also. Heads which are not selected are disconnected from the read bus by diodes which are back biased at 3.5 volts and are disconnected from the write bus by diodes which are back biased by a voltage from 1/2 to 15 volts, depending on the state of the writer.

In this manner it is possible to connect any of the bit sense amplifiers to a head for the same bit number in one of 32 fields, to connect the writer to one of the remaining 31 fields, and to have the remaining 30 fields back biased. Note that the common write bus for a bit is essentially coupled to a read bus by many back biased diodes. This coupling results in large noise spikes being induced in the read bus at write time. Because of the recording technique and timing used within the system, however, it is possible to strobe information from the sense amplifier before the write strobe is created, thereby storing the data in the out buffer before the large write transients occur.

Power Supply and Distribution

The parallel drum operates from a single source of 115-volt, 60-cycle, single-phase power. Control and overload protection for this power within the machine are exercised by a Type 813 Power Control. Operation of the power control can be controlled by the REMOTE ON/OFF/ LOCAL ON switch located on the indicator panel at the front of the machine, or by means of a contact closure provided from the computer when the computer is energized. The ac output of the power control operates the two cabinet fan motors, the two Type 728 Power Supplies, and the drum motor. Primary ac voltage is also supplied to a step down transformer through the normally closed contacts of a time-delay relay or (after the relay time has expired) through a voltage dropping resistor. This configuration provides a heater voltage to the bimetal strips in the drum of approximately 25 vac for the first 20 minutes of drum operation (current supplied to the transformer primary through the normally closed relay contacts) and supplies a heater voltage from 19.5 to 20.0 vac when the drum is ready for data transfers (current supplied to the primary of the transformer through the voltage dropping resistor). The primary of this transformer is also protected by a 5-ampere indicating type fuse and is interrupted if the vane

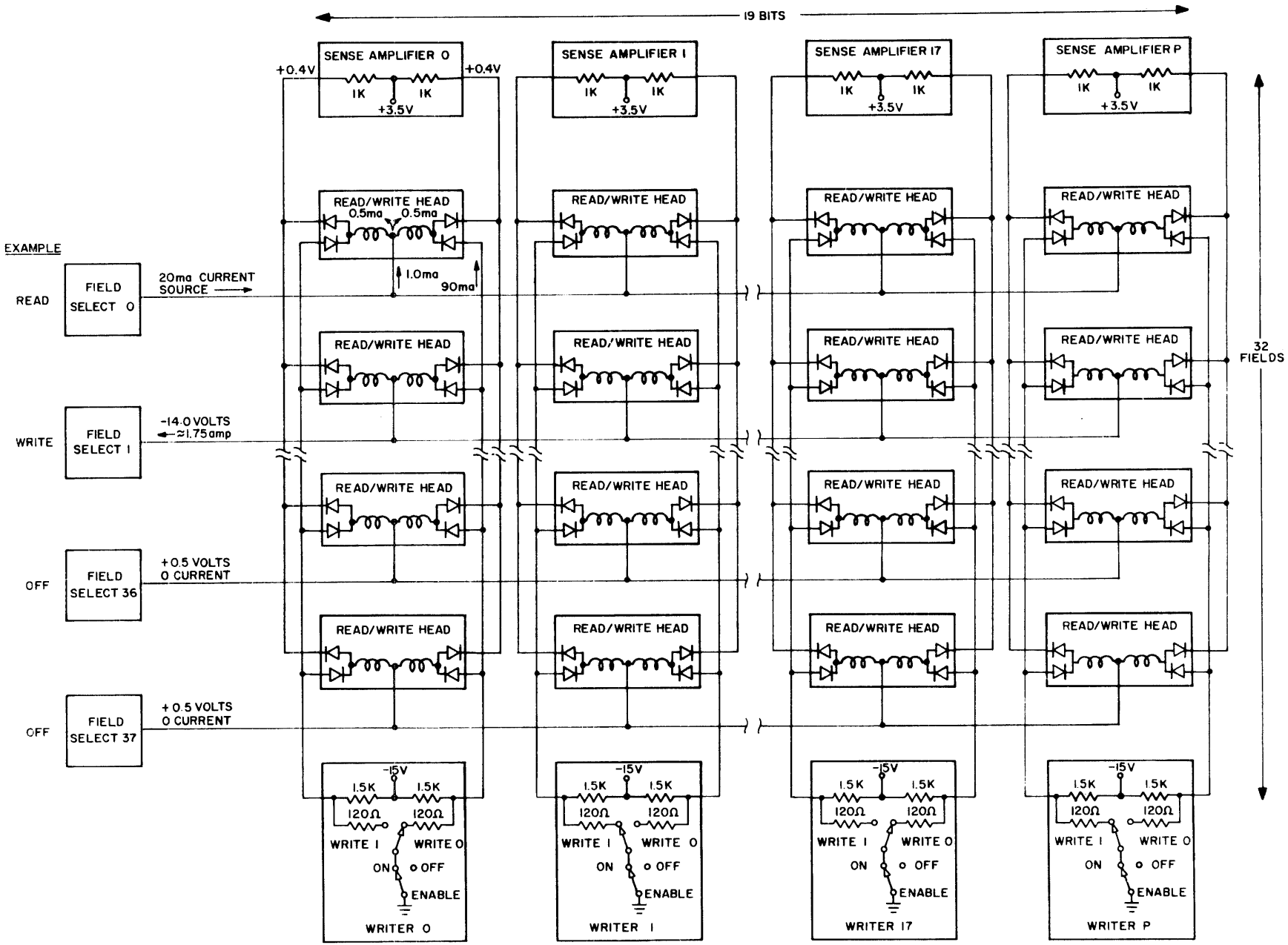


Figure 2-2 Data Head Selection

air switch on the top of the drum housing opens, indicating low drum speed. The bimetal heater voltage is supplied in parallel to all of the bimetal strip heaters. The - 15 volt output of the Type 728 Power Supply, which operates the indicator panel, is controlled by the normally open contact of the 20-minute time-delay relay. Therefore, the indicators do not light until the drum has been energized for 20 minutes, at which time the drum has reached synchronous speed and thermal stability and is ready to transfer data. All ac and dc wiring within the parallel drum is indicated on engineering drawing PW-D-23-0-8 and on Figure 2-3.

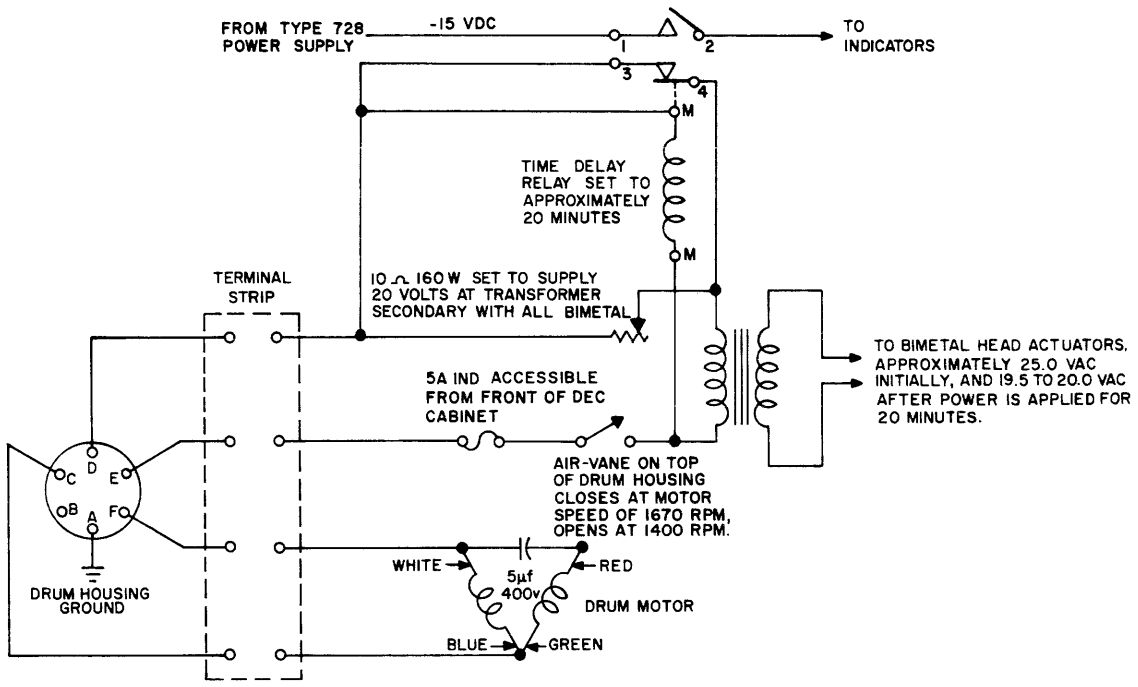


Figure 2-3 Drum Power Circuit

The normal module operating voltages of + 10 and - 15 vdc are supplied to each rack of logic through a color-coded connector at the right side of each rack, as seen from the module side. Marginal-check terminals on these connectors are connected in common on all module mounting panels within the machine so that the + 10 volt mc can be used to marginal check the + 10 vdc voltages supplied to any mounting panel within the machine. The color-coding of these connectors is as follows, from top to bottom.

a. Green, +10 v mc from the computer
b. Red, + 10 vdc internal supply
c. Black, ground
d. Blue, - 15 vdc internal supply
e. Yellow, - 15 vdc external marginal-check supply (unused)

Three single-pole double-throw switches at the end of each rack of logic allow selection of either the normal internal + 10 vdc power or an external marginal-check source of power for distribution to the logic. The top switch selects the + 10 vdc supply routed to terminal A of all modules in that mounting panel. In the down position the fixed internal + 10 volt supply connected to the red terminal is routed to all of the modules; in the up position the marginal-check voltage connected to the green terminal is supplied to terminal A of all of the modules. The center switch performs the same selection as the top switch for connection of a + 10 volt supply to terminal B of all modules within a mounting panel. The bottom switch selects the - 15 volt supply to be routed to terminal C of all modules in a mounting panel. In the down position the fixed - 15 volt output of the internal power supply, received at the blue terminal, is supplied to all of the modules; in the up position a marginal-check voltage, supplied by an external supply connected to the yellow terminal, is supplied to terminal C of all modules. However, since the - 15 volt supply is the collector load potential in most DEC modules and is normally clamped at - 3 volts, marginal checking of this source has very little effect upon the logical operation of the machine. Marginal checking of this line, however, does vary the output of modules containing an output pulse amplifier, and is therefore useful in checking the operation of circuits employing pulse amplifiers or in checking the operation of circuits which follow them.

READ-WRITE CYCLE

Three computer IOT instructions initialize and initiate a complete transfer. These instructions are the DIA or DBA, DWC, and DCL, and must occur in this order. Each of these instructions causes two 0.4 microsecond pulses to be supplied to the parallel drum, one at computer 7 time (TP7) and one at computer 10 time (TP10). The DIA instruction, for example, produces a DIA 7-4 pulse at computer 7 time and a DIA 10-4 pulse at computer 10 time. Normally the pulse supplied at computer 7 time clears a register and the pulse at computer 10 time, which is approximately 2.2 microseconds later, strobes information into or out of registers. In the three instruction sequence mentioned previously, the first command pulse received is a DIA 7-4 pulse, which clears all necessary control flip-flop registers. The DIA 10-4 pulse loads the read control flip-flop, loads the RFB, and loads the IL from the contents of the computer IO register. This same operation occurs during a DBA instruction except that the DBA 7-4 pulse also sets the DBA sync flip-flop. The second instruction clears the WC with a DWC 7-4 pulse,

then loads the write control flip-flop, loads the WFB, and loads the WC from the contents of the computer IO register by means of the DWC 10-4 pulse. The third instruction increments the contents of the WC by one and clears the DCL by means of a DCL 7-4 pulse, then loads the contents of the computer IO register into the DCL and sets the busy flip-flop by means of the DCL 10-4 command pulse. This command pulse also initiates operation of the 250-microsecond delay (Type 4301 module at location 1F11) which eventually initiates the data transfer. After giving the DCL instruction, the computer continues in the main program. Engineering drawing 1 shows the timing of control signals and the flow of information during a transfer.

The 250-microsecond delay is necessary for the read and write field select circuits to assume their respective states. Settling time for the readers is between 50 and 100 microseconds. Therefore, the 250-microsecond delay allows all transients to settle before the transfer commences. When the 250-microsecond delay expires, the transfer request (TRA) flip-flop is set to 1, and the timing of the transfer is now in the control of the drum timing and control elements.

Every 8.5 microseconds the timing element produces a phase A pulse which increments the contents of the DC so that it keeps track of the angular position of the drum. When the drum position arrives at the drum address or initial location of the transfer, the DC=IL signal is produced. The next phase A pulse sets the request (RQ) flip-flop to the 1 state. The request flip-flop then signals the memory control that a transfer cycle is requested by the drum. The change of state of the request flip-flop from 0 to 1 sets the error sync flip-flop to the 1 status. When the request is honored by memory control, the address acknowledge pulse is returned from the memory control to the drum. This pulse immediately clears the error sync flip-flop. If the request is honored within approximately 5.1 microseconds, the next phase A pulse sets the active (ACT) flip-flop to the 1 state, and data transfers occur within the current clock cycle. If the address acknowledge pulse is not received more than 2 microseconds before the phase A time occurs, indicating that the request was not honored by memory control, the request flip-flop is cleared and the parallel drum goes into a waiting loop. The TRA flip-flop remains in the 1 status and again initiates a request when the DC=IL signal is generated. This takes one drum revolution or approximately 35 milliseconds.

Since the drum usually has the highest request priority, a drum request is normally honored by memory control. When a drum request is made, memory control usually completes the current cycle and then honors the drum request by supplying an address acknowledge pulse after a period of from 0.1 to 5.1 microseconds.

On receipt of an address acknowledged pulse, the in buffer and the out buffers are cleared. After a period of 1 microsecond the error sync flip-flop is cleared, indicating that an address acknowledge pulse has been received. At this time the DCL is incremented by 1. Information which has been read out of core memory is available in the memory buffer register and is strobed into the drum in buffer via the pulsed bus transceiver 1.4 microseconds after the address acknowledge pulse is received. Memory control also supplies the read restart (RD RS) signal which clears the read parity flip-flop approximately 1.4 microseconds after the address acknowledged pulse is received. At the next phase A time the active flip-flop is set to 1 and the actual transfer of information to and/or from the drum surface commences.

When the active flip-flop is set to 1, the interface timing pulses, phase 1 through phase 3, are generated by the timing element. At phase 1 time the read strobe pulse is produced to read information from the read field selected and set it into the out buffer. The write strobe begins 0.1 microseconds later and immediately writes the contents of the in buffer on the drum surface and increments the contents of the WC by 1. At phase 2 time the writing operation is completed and the in buffer is cleared. At phase 3 time the out buffer, which stored the information previously read, sends the information back to memory control and to the in buffer by means of the pulsed bus transceiver. At this time the write restart (WR RS) pulse is sent to memory control, allowing the word which has just been placed on the pulsed bus transceiver MB lines to be rewritten in the computer core memory. As the word that was previously read from the drum surface is now contained in the in buffer, the parity formation element receives this information to generate the write parity bit. At phase 4 time the write parity bit just formed is compared with the contents of the read parity flip-flop. If the read parity bit and the write parity bit are not equal, the parity error (PE) flip-flop is set to 1 at phase 4 time.

At the start of the next drum clock cycle, the phase A pulse sets the error sync flip-flop, and the drum waits for an address acknowledge pulse to continue in a normal transfer.

If the most significant bit of the word counter overflowed during the previous transfer, that is, WC_6 is incremented to the point where it changes from the 1 to the 0 state, the request flip-flop is immediately cleared. At the next phase A time following clearing of the request flip-flop, the active flip-flop is cleared, the busy flip-flop is cleared, and the sequence break signal return pulse is supplied to the memory control to terminate the transfer. If the WC did not overflow during the previous transfer, the request flip-flop remains in the 1 status, and the

memory control passes into the first half of the next memory cycle. The cycle repeats as before; an address acknowledge signal must be received to continue the transfer. If the address acknowledge is not received within the allotted time, the next phase A pulse sets the transfer error flip-flop and clears the request flip-flop. The subsequent phase A pulse clears the active flip-flop, generates a sequence break signal return pulse, and clears the busy flip-flop. This action terminates an unsuccessful transfer which should not occur in normal operation, and so is indicative of equipment malfunction.

If the address acknowledge signal is received, the transfer continues. When the correct number of words has been transferred, the WC_6^0 overflows and clears the request flip-flop. At the subsequent phase A time the active flip-flop is cleared, a sequence break signal return pulse is generated and returned to the computer, and the busy flip-flop is cleared indicating the end of a successful transfer.

At the end of any transfer the DRA instruction must be executed and the status of the error flip-flops must be evaluated by the program before the data transferred can be deemed valid. During the DRA instruction, the inclusive OR of the status of the parity error and transfer error flip-flops is set into the contents of the computer IO register bit 0, and the contents of the parity error and the contents of the transfer error are set directly into the contents of the computer IO register bits 1 and 2, respectively. A parity error indicates that data bits have been picked up or dropped out during the transfer. If the address acknowledge pulse is not received for the initial word of a transfer, the transfer is never undertaken. This condition is indicated by both the TRA and ERROR SYNC indicators being lit. If the address acknowledge pulse is not received at any time during a transfer, both the TE indicator and the ERROR SYNC indicator are lit. This is an abnormal condition which indicates equipment malfunction.

READ ONLY CYCLE

A read only cycle is similar to a read-write cycle except that the information is read out of the computer core memory and placed in the contents of the in buffer. Generation of the write current is inhibited and no writing takes place. At phase 2 time the in buffer is cleared and the information that was received from core memory is lost, and the contents of core memory remains all zeros. New information which is read from the drum surface is then available in the out buffer and is sent back to the memory control at the proper time and is written into

the vacant core memory address. Parity checking occurs during a read only cycle. All timing remains the same as in the read-write cycle.

WRITE ONLY CYCLE

The write only cycle is similar to the read-write cycle. However, at phase 1 time the word which was read out of core memory exists in the in buffer and is transferred into the out buffer, instead of strobing new information from the drum surface into the out buffer. Writing takes place in the normal fashion, and the in buffer is cleared at the end of the write strobe pulse. At phase 3 time the contents of the out buffer are sent back to memory control, thereby, restoring the word in core memory which was previously read (from the same address). No parity checking occurs during a write only cycle.

SECTION 3

INTERFACE

All logic signals which pass between the PDP-1D computer or the memory control and the Type 23 Parallel Drum are standard DEC levels or standard DEC pulsed. A standard DEC level is either ground potential (0.0 to - 0.3 volts) or - 3 volts (- 3.0 to - 4.0 volts). Standard DEC pulses are 2.5 volts in amplitude (2.3 to 3.0 volts) and are referenced to the standard negative level. The standard pulse duration is 70 nanoseconds for pulses originating in Series 1000 modules, and 400 nanoseconds for Series 4000 modules.

In addition to the logic signal inputs a contact closure in the computer power control circuit provides the remote turn on signal to the power supply and distribution network in the parallel drum. In normal operation this signal is used to energize or de-energize the parallel drum from the computer. The effect of this signal can be disabled during maintenance operations to control power application and removal via a switch on the indicator panel of the parallel drum. The adjustable + 10 volt mc voltage from the computer marginal check panel is also supplied to the power supply and distribution element in the parallel drum to simplify drum maintenance.

Interface signals which pass between the parallel drum and the PDP-1D are listed in Tables 3-1 and 3-2 and on engineering drawing CL-A-23-0-16. All of the interface signals which flow between the parallel drum and the memory control are listed in Tables 3-3 and 3-4. The memory buffer register connections are made to the inside (handle) end of the pulsed bus transceiver in the drum and are shown on zone 1B of engineering drawing BS-D-23-0-3. All other interface connections from memory control are made to connectors 1E01 or 1E02 on the drum. All interface signal connections between the drum and the PDP-1D are made to connector 2C01 on the drum.

Note that IO input signal levels to the WFB, RFB, DCL, and WC must be present for at least 1 microsecond before receipt of the IOT pulse which strobes the data contents into the flip-flops. This delay is required to allow set up of the capacitor-diode gate at the input of each flip-flop on the Type 4217 modules.

TABLE 3-1 INPUTS TO DRUM FROM PDP-1D

Signal Name	Symbol	From PDP-1D Logic	To Parallel Drum		
			Connector	Logic	Drawing
IO_0		IO REG	2C01-1	WRITE, WFB READ, RFB	5 5
IO_1		IO REG	2C01-2	WRITE, WFB READ, RFB	5 5
IO_2		IO REG	2C01-3	DCL READ, RFB WRITE, WFB	6 5 5
IO_3		IO REG	2C01-4	DCL WRITE, WFB READ, RFB	6 5 5
IO_4		IO REG	2C01-5	DCL WRITE, WFB READ, RFB	6 5 5
IO_5		IO REG	2C01-6	DCL WRITE, WFB READ, RFB	6 5 5
IO_6		IO REG	2C01-7	DCL, IL, WC	6
IO_7		IO REG	2C01-8	DCL, IL, WC	6
IO_8		IO REG	2C01-9	IL, WC	6
IO_9		IO REG	2C01-10	IL, WC	6

TABLE 3-1 INPUTS TO DRUM FROM PDP-1D (continued)

Signal Name	Symbol	From PDP-1D Logic	To Parallel Drum		
			Connector	Logic	Drawing
IO_{10}	◇—	IO REG	2C01-11	IL, WC	6
IO_{11}	◇—	IO REG	2C01-12	IL, WC	6
IO_{12}	◇—	IO REG	2C01-13	IL, WC	6
IO_{13}	◇—	IO REG	2C01-14	IL, WC	6
IO_{14}	◇—	IO REG	2C01-15	IL, WC	6
IO_{15}	◇—	IO REG	2C01-16	IL, WC	6
IO_{16}	◇—	IO REG	2C01-17	IL, WC	6
IO_{17}	◇—	IO REG	2C01-18	IL, WC	6
DIA 7-4	▶	IO CONTROL	2C01-39	IL CONTROL	6 2
DIA 10-4	▶	IO CONTROL	2C01-40	IL READ, RFB	6 5
DWC 7-4	▶	IO CONTROL	2C01-41	WC	6
DWC 10-4	▶	IO CONTROL	2C01-42	WC WRITE, WFB READ, RFB	6 5 5

TABLE 3-1 INPUTS TO DRUM FROM PDP-1D (continued)

Signal Name	Symbol	From PDP-1D Logic	To Parallel Drum		
			Connector	Logic	Drawing
DCL 7-4	→	IO CONTROL	2C01-43	DCL WC	6 6
DCL 10-4	→	IO CONTROL	2C01-44	DCL CONTROL	6 2
DRA 7-4	→	IOT	2C01-45	CONTROL	2
DBA 7-4	→	IOT	2C01-46	CONTROL	2
+10V MC	→	MARGINAL CHECK	2C01-47	PS, DIST	8
REMOTE ON	→	POWER CONTROL	2C01-48 2C01-49	PS, DIST	8

TABLE 3-2 OUTPUTS FROM DRUM TO PDP-1D

Signal Name	Symbol	From Parallel Drum			To PDP-1D Logic
		Logic	Drawing	Connector	
ERROR STATUS	◆→	CONTROL	2	2C01-19	IO CONTROL
PE	◆→	CONTROL	2	2C01-20	IO CONTROL
TR ER	◆→	CONTROL	2	2C01-21	IO CONTROL

TABLE 3-2 OUTPUTS FROM DRUM TO PDP-1D (continued)

Signal Name	Symbol	From Parallel Drum			To PDP-1D
		Logic	Drawing	Connector	Logic
BUSY	◆→	CONTROL	2	2C01-22	STATUS REG
DC => IO STROBE	→	CONTROL	2	2C01-37	IM
SBS RETURN	→	CONTROL	2	2C01-38	SEQ BREAK

TABLE 3-3 INPUTS TO DRUM FROM MEMORY CONTROL

Signal Name	Symbol	From Memory Control Logic	To Parallel Drum		
			Connector	Logic	Drawing
RD RS	→	MBI	1E1C	Parity Check	2
ADRS ACK	→	MBI	1E1B	IB PBT	3 3
MB_0	→	MBI	1030-1	PBT	3
MB_1	→	MBI	1030-2	PBT	3
MB_2	→	MBI	1030-3	PBT	3
MB_3	→	MBI	1030-4	PBT	3

TABLE 3-3 INPUTS TO DRUM FROM MEMORY CONTROL (continued)

Signal Name	Symbol	From Memory Control Logic	To Parallel Drum		
			Connector	Logic	Drawing
MB_4	→	MBI	1030-5	PBT	3
MB_5	→	MBI	1030-6	PBT	3
MB_6	→	MBI	1030-7	PBT	3
MB_7	→	MBI	1030-8	PBT	3
MB_8	→	MBI	1030-9	PBT	3
MB_9	→	MBI	1030-10	PBT	3
MB_{10}	→	MBI	1030-11	PBT	3
MB_{11}	→	MBI	1030-12	PBT	3
MB_{12}	→	MBI	1030-13	PBT	3
MB_{13}	→	MBI	1030-14	PBT	3
MB_{14}	→	MBI	1030-15	PBT	3
MB_{15}	→	MBI	1030-16	PBT	3
MB_{16}	→	MBI	1030-17	PBT	3
MB_{17}	→	MBI	1030-18	PBT	3

TABLE 3-4 OUTPUTS FROM DRUM TO MEMORY CONTROL

Signal Name	Symbol	From Parallel Drum Logic	To Memory Control		
			Connector	Logic	Drawing
DCL_2^0		DCL	1E01K	MBI	6
DCL_2^1		DCL	1E01L	MBI	6
DCL_3^0		DCL	1E01M	MBI	6
DCL_3^1		DCL	1E01N	MBI	6
DCL_4		DCL	1E02B	MBI	6
DCL_5		DCL	1E02C	MBI	6
DCL_6		DCL	1E02D	MBI	6
DCL_7		DCL	1E02E	MBI	6
DCL_8		DCL	1E02F	MBI	6
DCL_9		DCL	1E02H	MBI	6
DCL_{10}		DCL	1E02K	MBI	6
DCL_{11}		DCL	1E02L	MBI	6

TABLE 3-4 OUTPUTS FROM DRUM TO MEMORY CONTROL (continued)

Signal Name	Symbol	From Parallel Drum Logic	To Memory Control		
			Connector	Logic	Drawing
DCL_{12}	◆—	DCL	1E02M	MBI	6
DCL_{13}	◆—	DCL	1E02N	MBI	6
DCL_{14}	◆—	DCL	1E02P	MBI	6
DCL_{15}	◆—	DCL	1E02R	MBI	6
DCL_{16}	◆—	DCL	1E02T	MBI	6
DCL_{17}	◆—	DCL	1E02U	MBI	6
RQ	◆—	CONTROL	1E01F	MBI	2
RD REQ	◆—	CONTROL	1E02V	MBI	2
WR REQ	◆—	CONTROL	1E02W	MBI	2
WR RS	—▶	TIMING	2E01D	MBI	2
MB_{0-17}	—▶	PBT	See Table 3-3	MBI	3

SECTION 4

INSTALLATION AND OPERATION

SITE REQUIREMENTS

The installation site must provide floor space at least 47 inches wide and 28 inches deep to accommodate the parallel drum. At least 9 inches must be provided in front of the cabinet and 15 inches at the back of the cabinet to allow opening of the doors for maintenance.

A source of 115-volts (±17 volts), 60 cycle, single-phase power must be supplied by the site. This source must be capable of supplying the 10.0-ampere starting surge current and 9.0-ampere running current required by the drum.

Ambient temperature at the installation site can vary between 32 and 105 degrees Fahrenheit (0 to 41 degrees centigrade) without deleterious effect upon equipment operation. For normal operation an ambient temperature range from 70 to 85 degrees Fahrenheit is recommended.

Shipping weight of a Type 23 Parallel Drum is approximately 1090 pounds.

SIGNAL AND POWER CONNECTIONS

Signal connections to the Type 23 Parallel Drum from the PDP-1D are made at connector 2C01 on the plug panel at the front of the machine. Signal connections to the drum from the memory control are made at connectors 1E01 and 1E02 at the front of the machine. To mate with these connectors, a cable should contain an Amphenol connector of the 115-114P series with a housing 1391 and wire clamp 3057. Signal cable length should not exceed 25 feet. The input and output signals are defined in Tables 3-1 and 312 and their wiring connections are given on sheets 1 and 2 of the engineering drawing A-24614. Data connections to the drum from the memory control are made to the back of the Type 1665 Pulsed Bus Transceiver at location 1H24. The data cable must be 18-conductor coaxial, terminated in a Type 1031 or 1032 module.

A grounded, three-wire power cable is permanently attached to the machine. A standard 3-prong male power plug at the end of this cable allows connection to a power source 18 feet from the cabinet.

CONTROLS AND INDICATORS

Manual control of the parallel drum is exercised by means of switches on the indicator panel (1A) and on the field lockout switch panel (2D). Visual indications of the machine status and register contents is given on the indicator panel and the auxiliary indicator panel (2A) shown in Figure 4-1. The function of all machine controls and indicators is given in Table 4-1.

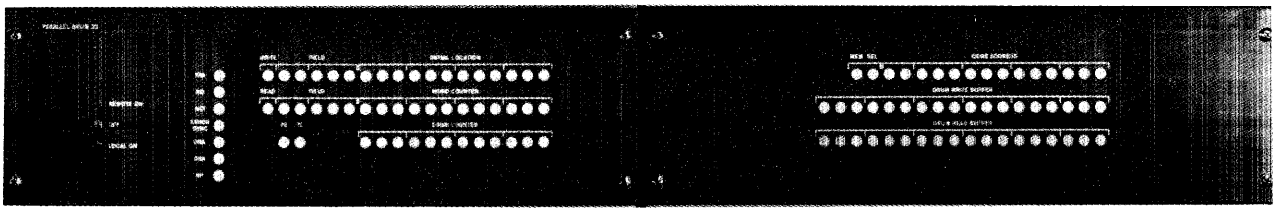


Figure 4-1 Indicator Panels

TABLE 4-1 CONTROLS AND INDICATORS

Control or Indicator	Function
	Indicator Panel
REMOTE ON/OFF/LOCAL ON switch	Allows local or remote control of machine energization. In the REMOTE ON position the machine is energized by a contact closure in the computer. The OFF and LOCAL ON positions function as a normal power switch.
TRA indicator	Lights to acknowledge receipt of DCL transfer IOT pulses and indicates that the drum is waiting for the drum counter to arrive at the starting address of the transfer specified by the contents at the initial location register.

TABLE 4-1 CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
RQ indicator	Lights to indicate that a request signal has been sent to the memory control to request a transfer. This indicator remains lit for the duration of a transfer.
ACT indicator	Lights to indicate that the drum is actively transferring data with the memory control.
ERROR SYNC indicator	Lights to indicate the 1 status of the error sync flip-flop. This flip-flop is set at the time the request signal is sent to the memory control and should be turned off within 6 microseconds by receipt of an address acknowledged signal from the memory control. If this indicator is lit and the TRA indicator is lit, the first acknowledged pulse has not been received from the memory control and no transfer has occurred. If this indicator is lit and the TE indicator is lit, a transfer was started and erroneously interrupted.
DRA indicator	Lights to indicate the binary 1 status of the DRA sync flip-flop. This flip-flop is set to 1 by receipt of a DRA 7-4 pulse which causes the current address contained in the drum counter to be strobed into the input-output (IO) register of the PDP-1D, therefore allowing a rapid transfer of 4096 words beginning at an address determined by the current drum position and a program-added constant.
DBA indicator	Indicates the binary 1 status of the drum break address (DBA) sync flip-flop. This flip-flop is set to 1 by receipt of a DBA 7-4 IOT pulse from the PDP-1D. The next phase A clock pulse clears this flip-flop and causes generation of a sequence break signal return which is supplied to the PDP-1D when the drum counter equals the location register. This pulse also clears the busy flip-flop.

TABLE 4-1 CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
RP indicator	Lights to indicate the binary 1 status of the read parity flip-flop which stores the parity bit just read from the drum. The contents of this flip-flop are compared with a reformed parity bit for the word just read as a parity error check.
WRITE and FIELD indicators	Light to indicate the 1 status of the write and write-field buffer flip-flops which are set by the contents of bits 0-5 of the IO register during DWC 10-4 instruction. The contents of the buffer indicate the write field currently selected.
READ and FIELD indicators	Light to indicate the binary 1 status of the read flip-flop and the read field buffer register flip-flops. These flip-flops are set by the contents of IO register bits 0-5 during a DIA 10-4 instruction. The contents of the buffer indicate the read field currently selected.
PE indicator	Lights to indicate that the machine has detected a read parity error (bits have been picked up or dropped out of the word just read, the READ BAD PARITY pushbutton has been pressed prior to the transfer, or the parity formation or check circuits are defective).
TE indicator	Lights to indicate that the machine has detected a transfer error in which a transfer was interrupted before it was completed.
INITIAL LOCATION indicators	Light to indicate the binary 1 status of bits in the location register. The word in the location register specifies the first address of a transfer.
WORD COUNTER indicators	Light to indicate the binary 1 status of the word counter flip-flops. The contents of the word counters specify the number of words to be transferred.

TABLE 4-1 CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
DRUM COUNTER indicators	Light to indicate the binary 1 status of bits of the drum counter. The contents of the drum counter indicates the angular position of the drum as divided into 4096 positions.
	Auxiliary Indicator Panel
MEM SEL indicators	Light to indicate the binary 1 status of the two most significant bits of the drum core location counter. This number specified the bank of computer core memory to or from which data is transferred with the drum.
CORE ADDRESS indicators	Light to indicate the binary 1 status of bits in the drum core location counter. This number indicates the address of core memory to or from which data is being transferred.
DRUM WRITE BUFFER indicators	Light to indicate the binary 1 status of each bit of the in buffer. The contents of this register are written on the drum during a write operation and are used to form the parity bit. During read operation, the contents of this register are used to generate a parity bit which is compared with the contents of the read parity flip-flop for parity error checking.
DRUM READ BUFFER indicators	Light to indicate the binary 1 status of bits of the out buffer. The contents of this register indicate the contents of the word just read from the drum during a read operation. During a write operation, the contents of this register are returned to the memory control to restore the same information core memory.
	Field Lockout Switch Panel
WRITE FIELD LOCKOUT SWITCHES FO through F37	Each switch allows 1 field (4096 words) to be inhibited during writing. Therefore, the information stored in a field cannot be accidentally destroyed by writing new information over that presently contained in the field.

TABLE 4-1 CONTROLS AND INDICATORS (continued)

Control or Indicator	Function
WRITE BAD PARITY pushbutton	Allows the first word of the next transfer to be written with an incorrect parity bit so that a routine can check the operation of the error parity circuits. A programmer can use this switch to test his error check programs.

EQUIPMENT TURN-ON AND TURN-OFF

Operation of the Type 23 can be controlled locally by operation of a switch, or remotely from a circuit closure in the computer. Control point is selected at the REMOTE ON/OFF/ LOCAL ON switch on the indicator panel. In normal use this switch is left in the REMOTE ON position. For maintenance operations this switch is set to the LOCAL ON position to apply power and to the OFF position to remove power. Note that the circuit breaker on the Type 813 Power Control must be in the ON position to allow either local or remote control of primary power in the parallel drum.

SECTION 5

PROGRAMMING

The PDP-1D IOT instructions which operate the Type 23 Parallel Drum are listed in Table 5-1. Octal codes containing X's indicate bits which are not applicable and can be either ones or zeros. Octal codes specifying zeros must contain zeros.

TABLE 5-1 INSTRUCTIONS

Octal Code	Mnemonic Code	Name and Function
72XX61	DIA	Drum Initial Address. Load read control, read field buffer, and initial location. $C(IO)^{1}_{0} \Rightarrow C(Read)^{1}$ to specify reading $C(IO)^{1}_{1-5} \Rightarrow C(RFB)^{1}_{1-5}$ to select read field $C(IO)^{1}_{6-17} \Rightarrow C(IL)^{1}_{6-17}$ to specify initial drum address.
72XX62	DWC	Drum Word Count. Load write control, write-field buffer, and word counter. $C(IO)^{1}_{0} \Rightarrow C(Write)^{1}$ to specify writing $C(IO)^{1}_{1-5} \Rightarrow C(WFB)^{1}_{1-5}$ to select write field $C(IO)^{0}_{6-17} \Rightarrow C(WC)^{1}_{6-17}$ to specify the number of words to be transferred.
72XX63	DCL	Drum Core Location. Load drum core location register with Memory Select and computer address of initial transfer; then initiate a transfer. The transfer begins when the drum reaches the address contained in the initial location register. When the transfer is complete, the drum clears the request flip-flop.

TABLE 5-1 INSTRUCTIONS (continued)

Octal Code	Mnemonic Code	Name and Function
72XX63 (cont'd)	DCL	$C(IO)^1_{2-17} \Rightarrow C(DCL)^1_{2-17}$ Bits IO^1_{2-3} select a memory bank as follows: Bank 0 = IO^0_2 and IO^0_3 Bank 1 = IO^0_2 and IO^1_3 Bank 2 = IO^1_2 and IO^0_3 Bank 3 = IO^1_2 and IO^1_3 Bits IO^1_{5-17} specify the address set into the memory control memory address register.
722061	DBA	Drum Break Address. Same as DIA instruction; when C(DC) = C(IL) the drum gives a sequence break return signal which indicates that the drum is ready to be reinitialized for another transfer and initiates a sequence break.
732062	DRA	Drum Request Address. The current drum address is transferred from the drum counter to the computer IO register. This number can then be incremented by 77_8 and set into the initial location counter during a DIA instruction for effecient transfer of 4096 words. $C(DC)^1_{6-17} \Rightarrow C(IO)^1_{6-17}$ $C(\text{Error Status}) \Rightarrow C(IO)^1_0$ $C(PE)^1 \Rightarrow C(IO)^1_1$ $C(TE)^1 \Rightarrow C(IO)^1_2$

A program to initialize and initiate a transfer of data between the memory control and the parallel drum consist of the instructions DIA, DWC, and DCL in that sequence. If the program uses the sequence break facilities of the computer, the program sequence is DBA, DWC, and DCL. When a transfer of 4096 words is planned, the DRA instruction can be used to save computer time. Since in a 4096-word transfer all addresses of a field are used, the transfer can begin and end at any address. Therefore, the DRA instruction is used to locate the current address of the drum. This address can be incremented by a predetermined value to form a number which represents the predicted drum address when the transfer will be initiated. The number added to the drum address is based on the drum changing addresses every 8.5 microseconds and is calculated to use drum time equal to the computer program time required to reach the DCL instruction. This number has been determined empirically, in a typical program, to be 77_8.

Transfers from 1 to 4096 words can be executed at a rate of one word every 8.5 microseconds, exclusive of program initialization and from address access time. Reading and writing can occur simultaneously, allowing the exchange of 4096 words in approximately 35 milliseconds.

After a program has been completed, the program must perform a DRA instruction and check the error status of the drum to assure the validity of the data transferred. If the error status is a 0, the transfer is valid and the program can continue or a new initialization can be initiated. If the error status is a 1, check the contents of PE and TE. If the PE is a 1, one or more data words were transferred incorrectly (bits were picked up or dropped out). If the TE is a 1, the transfer was terminated prematurely or was not enacted (addresses in core memory which were to be read from the drum or drum addresses which were to be written in may be cleared or contain previous information). In either case, repeat the transfer or commence drum corrective maintenance procedures.

SECTION 6

MAINTENANCE

Maintenance of the Type 23 Parallel Drum consists of procedures repeated periodically as preventive maintenance, and tasks performed in the event of equipment malfunction as corrective maintenance. The procedures presented here assume that the reader understands the function of the controls and indicators described in Table 4-1, and is familiar with PDP-1D and drum programming described in the PDP-1 handbook and in Section 5 of this manual. Maintenance activities require use of the equipment listed in Table 6-1, or equivalent, as well as the use of standard hand tools, cleansers, and test cables and probes.

TABLE 6-1 MAINTENANCE EQUIPMENT

Equipment	Manufacturer	Model
Multimeter	Triplett or Simpson	630-NA or 260
Oscilloscope	Tektronix	540 Series
Parallel Drum Diagnostic Program Tape	DEC	DEC-1-137-M
System Module Extender*	DEC	1954
System Module Puller*	DEC	1960

*One supplied with the equipment

If it is necessary to remove modules during either preventive or corrective maintenance, the Type 1960 System Module Puller should be used. Turn off all power before extracting or inserting modules. Carefully hook the small flange of the module puller over the center of the module rim, and gently pull the module from the mounting panel. Use a straight even pull to avoid damage to plug connections or twisting of the printed-wiring board. Since the puller does not fasten to the module, grasp the rim of the module to prevent it from falling. Access to controls on the module for use in adjustment, or access to points used in signal tracing can be gained by removing the module, connecting a Type 1954 System Module Extender into the mounting panel, and then inserting the module into the extender.

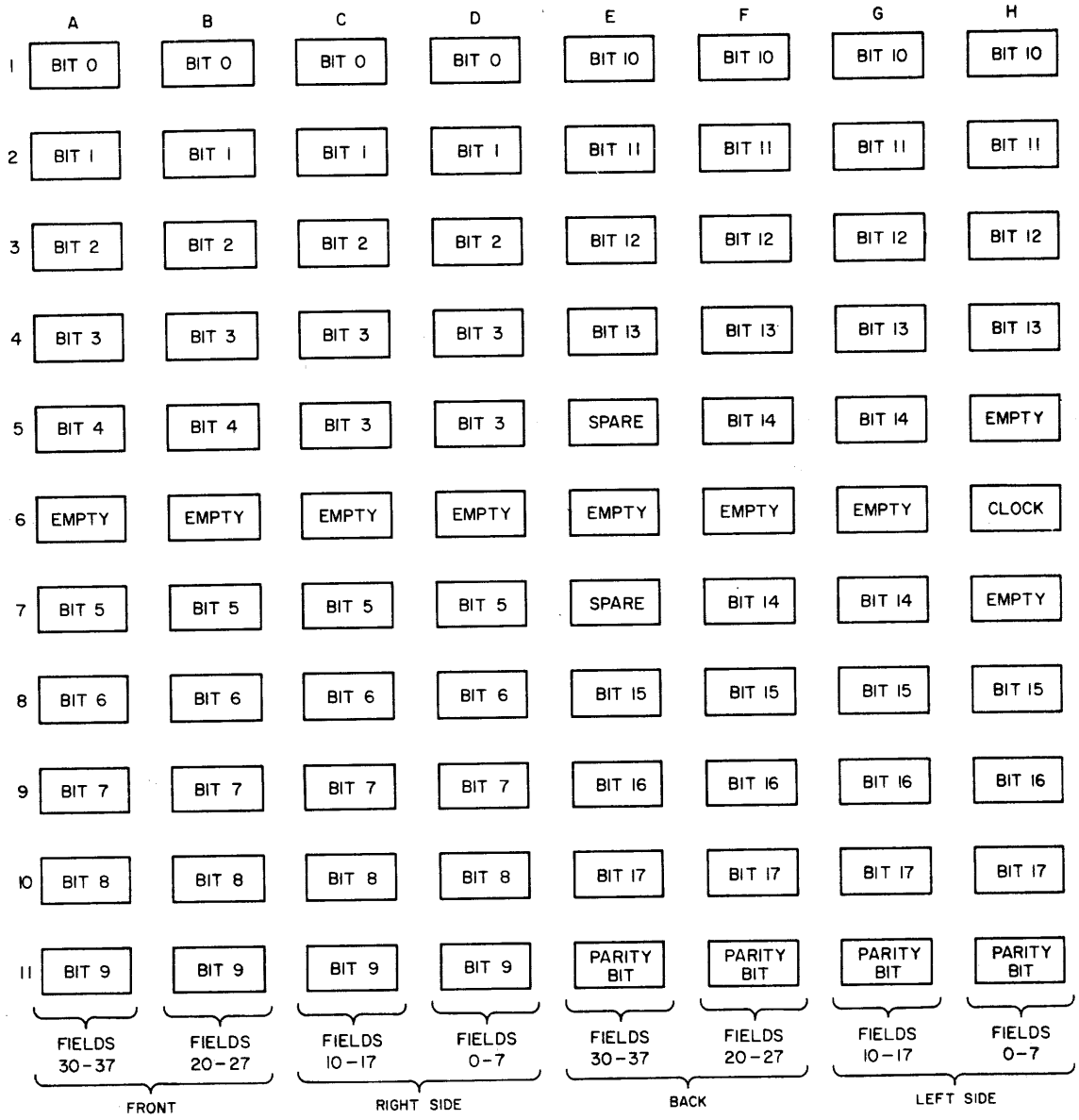
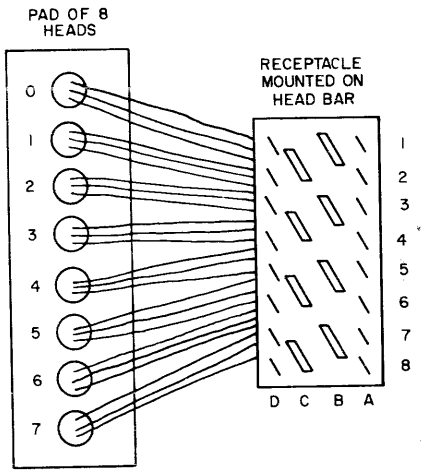


Figure 6-1 Pad Location

Drum Housing Component Locations and Wiring

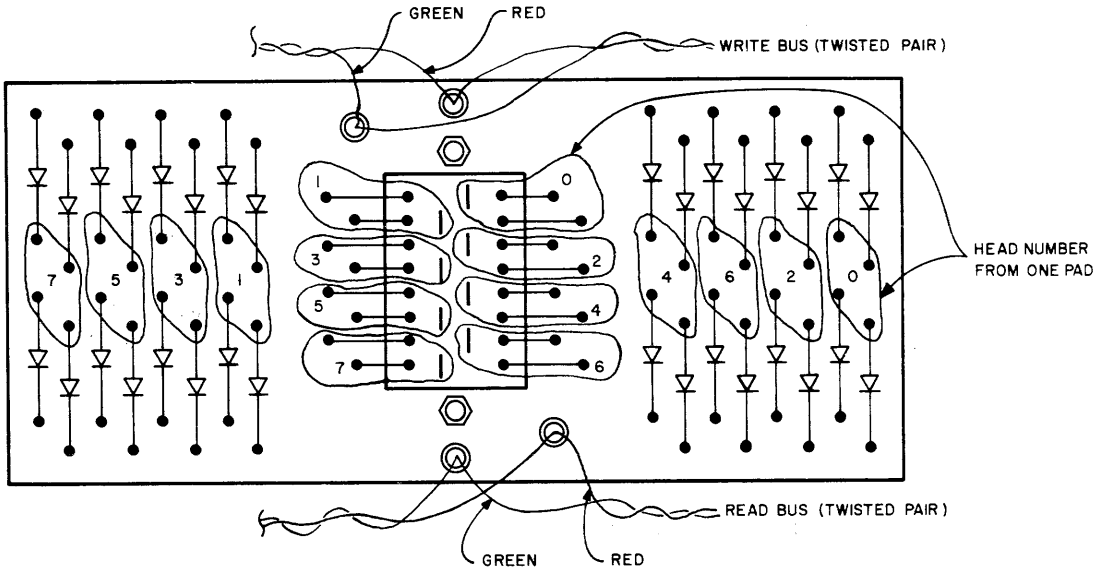
Around the surface of the drum shroud are 8 columns; each column contains 11 horizontal rows of read/write head mounting pads. The location of these pads is indicated in Figure 6-1. The columns are lettered A through H around the periphery of the drum and are suitably engraved. The rows are numbered from 1 through 11 from top to bottom, row 6 being used primarily to hold spare read/write heads. Four of these pads are required to contain 1 bit from each of the 32 fields. For example, to locate a pad containing bit 2 of field 12 it is necessary to remove the right side panel of the drum housing. By inspection, locate column C and count down for the third pad for bit 2. This pad contains bit 2 for fields 10 through 17.



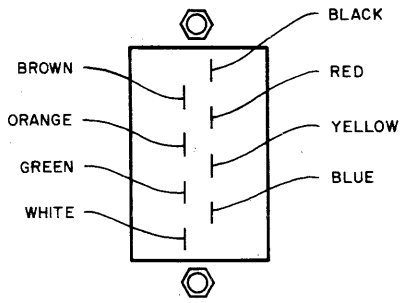
RECEPTACLE TERMINAL CONNECTIONS

HEAD	HEAD WIRING COLOR		
	RED	BLACK	GREEN
0	A2	B1	A1
1	D1	C2	D2
2	A4	B3	A3
3	D3	C4	D4
4	A5	B5	A6
5	D6	C6	D5
6	A7	B7	A8
7	D8	C8	D7

Figure 6-2 Head Wiring



a. DIODE AND GATE CONNECTIONS



b. DIODE BOARD PLUG WIRING OF FIELD SELECT LINES TO HEAD CENTER TAPS. EACH COLOR IS USED FOUR TIMES FOR THE 32 FIELDS

Figure 6-3 Diode Board Wiring

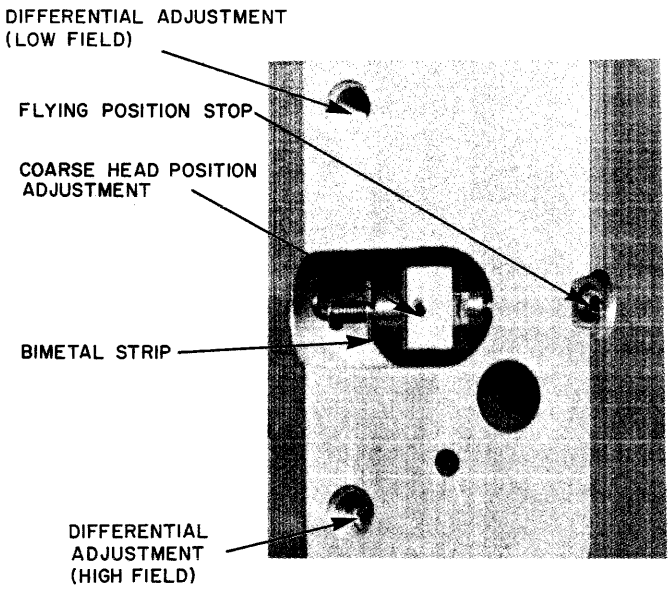


Figure 6-4 Read/Write Head Components

CAUTION

When a field selector is in the write state, -14.0 volts are applied to the centertap of the associated heads in the field. Since no current limiting exists, a short circuit between any potential more positive than -14.0 volts and an outside winding terminal or a write bus of a head selected in this manner results in destruction (opening) of the head winding and/or the select diodes.

Heads are numbered from 0 through 7 from top to bottom within a pad as indicated in Figure 6-2. This figure also indicates the wiring from the heads to the receptacle mounted on the head bar. This wiring connects to the plug in the center of the printed-wiring boards containing the head selection diode matrix. This wiring is color coded by field number so that black refers to field 0, 10, 20, or 30; brown to field 1, 11, 21, or 31; red to field 2, 12, 22, or 32, etc. This color coding and the wiring and positions of diodes within a head selection board are indicated in Figure 6-3. Note that there are 32 diodes on each board, 4 associated with each head. The field select lines attached to the centertap of each head are located by the wiring color code. At the top of each head selection board is a twisted pair of red and green wires which make up the write bus. At the bottom of each board is another red and green twisted pair of wires which are the read bus. Both these bus lines are tagged for identification.

The component parts of a pad of read/write heads are identified in Figure 6-4. The two differential adjustment screws provide a fine adjustment for the distance between the pad and the drum surface. Turning the upper differential adjustment of a pad counterclockwise moves one end of the pad toward the drum surface so that the displacement of head 0 is greatest, and the displacement of head 7 is the least. Differential movement of each head as the adjustment is turned is inversely proportional to the distance of each head from the adjusting screw. Therefore, turning the lower differential screw clockwise moves the pad nearer to the drum surface in a manner which increases the output voltage read from head 7 a greater amount than head 0. Turning both differential screws the same amount in the same direction should effect the output voltage from all heads by the same amount. The flying position stop limits the minimum head-to-drum surface distance. The course head position adjustment is factory-set so that field adjustment should not be necessary. The bimetal strip increases and decreases the pressure on the head, and therefore changes the head-to-drum surface distance as a function of internal drum housing temperature and drum speed of rotation.

At all times during any adjustment of a pad, listen carefully to assure that the pad does not come in contact with the drum surface. Any contact noise indicates a maladjustment. Immediately reverse direction of all adjustments and readjust the stop screw. After an adjustment has been made, stop the drum motor and listen for contact noise; then restart the motor and listen carefully again.

If it is necessary to gain access to the right side of the drum housing for maintenance of bits 0 through 9 of fields 0 through 7 or 10 through 17, the end panels of the parallel drum system cabinet must be removed. These panels are removed simply by lifting them above the frame on which they are hooked at top and bottom.

PREVENTIVE MAINTENANCE

Preventive maintenance consists of tasks performed prior to the initial operation of the equipment and periodically during its operating life to ensure that it is in satisfactory operating condition. Faithful performance of these tasks forestalls possible future failure by correcting minor damage and discovering progressive deterioration at an early stage. A log book used to record data found during the performance of each preventive maintenance task will indicate the rate of circuit operations deterioration and provide information to determine when components

should be replaced to prevent failure of the equipment. These tasks consist of mechanical checks, which include cleaning and visual inspections; checks of specific circuit elements such as the power supplies, clock and delay module timing, sense amplifiers, and magnetic heads; and marginal checks which aggravate border line conditions or intermittent failure so that they can be detected and corrected. All preventive maintenance tasks should be performed as a function of conditions at the installation site and the down-time limitations of equipment use. Perform the mechanical checks at least once each month or as often as required to allow efficient functioning of the air filters. All other tasks should be performed on a regular schedule, at an interval determined by the reliability requirements of the system. For a typical application a schedule of every four months or 700 equipment operating hours, whichever occurs first, is suggested.

Mechanical Checks

Assure good mechanical operation of the equipment by performing the following steps and the indicated corrective action for any substandard conditions found:

1. Clean the exterior and the interior of the equipment cabinet using a vacuum cleaner or clean cloths moistened in nonflammable solvent.

2. Clean the air filter at the bottom of each cabinet. Remove the filter by removing the fan and housing, which are held in place by two knurled and slotted captive screws. Wash the filters in soapy water, dry in an oven or by spraying with compressed gas, and spray with Filter-Kote (Research Products Corporation, Madison, Wisconsin) before replacing them in the cabinets.

3. Lubricate door hinges and casters with a light machine oil. Wipe off excess oil.

4. Visually inspect the equipment for completness and general condition. Repaint any scratched or corroded areas with DEC blue enamel, number 5150-S65.

5. Inspect all wiring and cables for cuts, breaks, fraying, deterioration, kinks, strain, and mechanical security. Tape, solder, or replace any defective wiring.

6. Inspect the following for secutiry: switches, knobs, jacks, connectors, transformers, fan, capacitors, lamp assemblies, etc. Tighten or replace as required.

7. Inspect all mounting panels of logic to assure that each module is securely seated in its connector.

8. Inspect power supply capacitors for leaks, bulges, or discolorations. Replace any capacitors giving these signs of malfunction.

Power Supply Checks

Check the output voltage and ripple content of the Type 728 Power Supplies, and assure that they are within tolerance. Use the multimeter to make the output voltage measurements without disconnecting the load. Use the oscilloscope to measure the peak-to-peak ripple content on dc outputs of the supplies. These supplies are not adjustable; so if the output voltage or ripple content is not within the tolerance specified, the supply is considered defective and troubleshooting procedures should be undertaken.

Check the +10 volt output between the black (-) and the red (+) terminals to assure that it is between 9.5 and 11.0 volts with less than 800 millivolts ripple. Check the -15 volt output between the black (+) and blue (-) terminals to assure that it is between 14.5 and 16.0 volts with less than 400 millivolts ripple. Note that the black terminals are common with the power supply chassis.

Timing Checks

There are four variable timing adjustments in the Type 23 Parallel Drum. Using the oscilloscope and referring to engineering drawings BS-D-23-0-2 and BS-D-23-0-4, check the timing of the Type 4401 Variable Clock at location 1F2, the Type 4301 Delay at location 1F11, and the two Type 1304 Delay modules at locations 1H6 and 2B3. If necessary, the timing of these modules can be adjusted by turning the potentiometer screw, which is accessible through a hole in the handle.

Check the timing of the variable clock to assure that standard DEC positive pulses occur at terminal 1F2F every 2 to 5 microseconds when the module is uninhibited. The clock can be

made free-running for this check by grounding the cathode of the diode input at terminal 1E83J. Be sure to remove this ground connection at the completion of this check or subsequent data transfers will be invalid.

Check the timing of the write strobe delay at location 1H6. The output at terminal 1H6J should be a negative level for 2.6 microseconds, occurring approximately every 8.5 microseconds as long as the drum is rotating. The oscilloscope can be synchronized on the negative leading edge of the clock pulse at location 1H5X when making this measurement.

Check the timing of the TRA delay at location 1F11 to assure that it is set for a minimum of 250 microseconds. To perform this check the delay can be initiated repeatedly by connecting the input terminal 1F11Y to the clock pulse at location 1H5X or the delayed clock pulse at 1H6E. The delay can be measured as the time between the negative initiating pulse and the negative output pulse at location 1F11E, or can be measured as a 250-microsecond negative level at output terminal 1F11J.

Check the timing of the index delay at location 2B3. This delay should be adjusted for a minimum delay which will place the index pulse at location 2B3E between successive phase A clock pulses, which can be observed at location 1H10V.

Drum Sense Amplifier Checks

The Type 1537 Drum Sense Amplifier modules (or readers) are checked for proper slice or threshold level by observing the amount the dc output base line at terminal S shifts with respect to ground when the input signal is received. The index reader at location 2B6, the clock reader at location 2B5, and the data readers at successive locations 2B7 through 2B25 are shown on engineering drawing BS-D-23-0-4. The clock track reader slice level output should shift by +100 millivolts. The index and data track sense amplifier slice level should shift by +275 millivolts. Adjustment of the slice level can be achieved by turning the potentiometer screw which is accessible through a hole in the module handle.

Index and Clock Head Spacing Checks

Mechanical adjustment of the index and clock heads can be checked by measuring the preamplifier output of the appropriate Type 1537 Drum Sense Amplifier modules at terminals 2B6S

(index) and 2B5S (clock). This output should be approximately 1.4 volts peak-to-peak, as measured on an oscilloscope. Adjustment of the head should be undertaken only if the preamplifier output is less than 1.0 volt, if the head has been replaced, or when operationl tests clearly indicate that it is required. Adjustment is made by means of the stop screw.

In any changes of the leads to the index or clock readers or to the index or clock heads, care must be taken to avoid any transients caused by soldering irons, static charges, etc. as they inadvertantly erase or destroy the prerecorded information on these tracks. The input terminals to the index and clock readers are normally protected with insulation to avoid inadvertant grounding. Grounding of any of the leads at the input of either the index or clock reader erases the prerecorded information on that track if drum power is on. No danger exists to the prerecorded information on the index and clock tracks when the parallel drum is de-energized and soldering of leads can be accomplished by means of a soldering iron containing an isolation transformer.

Data Head Spacing Checks

Check the mechanical spacing of each data head by measuring the output voltage of the appropriate Type 1537 Drum Sense Amplifier at the output of the preamplifier, which is terminal S. The readers for bits 0 through 17 are found in locations 2B8 through 2B25, respectively, and the parity bit is in location 2B7. The best method of making this check is to run a program in which patterns of all ones or alternate ones and zeros are written on a selected track, then continuously read as data is monitored on an oscilloscope. In this manner the contents of the read field buffer can be changed by means of the program to check the output from each head and all fields. If test data patterns are to be written during this check, and if the data on the drum surface is to be retained, it should be read into the computer core memory, the check performed on a specific field, and the data rewritten into that field at the end of the check. If the check is to be performed without the use of the computer, the read control flip-flop and the read field buffer flip-flops can be cleared or set manually by momentarily supplying a ground potential to the appropriate flip-flop output.

CAUTION

When a field selector is in the write state, -14.0 volts are applied to the centertap of the associated heads in the field. Since no current limiting exists, a short circuit between any potential more positive than -14.0 volts and an outside winding terminal or a write bus of a head selected in this manner results in destruction (opening) of the head winding and/or the select diodes.

Binary ones should produce an output of 1.4 volts peak-to-peak in any data patterns. Adjustment of the head should be undertaken only if the reader output is substantially less than 1.4 volts, if the head has been replaced, or when operational tests clearly indicate that it is required.

To determine if a pad of read/write heads needs be adjusted, connect the oscilloscope to terminal S of the appropriate reader module for the bit to be checked, and read and record the output obtained as the bit is read from each of the 7 heads selected by the contents of the read field buffer. The average output obtained from fields 0 through 3 should equal the average output obtained from fields 4 through 7. If fields 0 through 3 produce a lower output than fields 4 through 7, turn the upper differential screw clockwise or turn the lower differential screw counterclockwise. If a higher output is obtained from fields 0 through 3 than is obtained from fields 4 through 7, turn the upper differential screw counterclockwise or turn the lower differential screw clockwise. For example, if the lower numbered fields are providing an output lower than 1.4 volts and the higher fields are producing an output of no less than 1.4 volts adjust the upper screw clockwise. However, if the low numbered fields produce an average output which is no less than 1.4 volts and the high order fields produce an average output voltage much greater than 1.4 volts, turn the lower differential screw counterclockwise. If both high and low order fields produce average voltages which are approximately equal but less than 1.4 volts, turn the stop screw counterclockwise. If this does not result in higher average output signals, adjust both differential screws clockwise or counterclockwise by the same amount. After every adjustment rewrite the information passed by the adjusted pads and then read it again.

Marginal Checks

Marginal checks are performed to aggravate borderline circuit conditions within the control logic to produce observable faults. Therefore, conditions caused by marginal components can be corrected during scheduled preventive maintenance to forestall possible future equipment failure. These checks can also be used as a troubleshooting aid to locate marginal or intermittent components, such as deteriorating transistors.

The checks are performed by operating the logic circuits from an adjustable external power supply such as the +10v mc level adjusted at the computer marginal check switch panel or a separate external supply such as a DEC Type 730 Dual Variable Power Supply. Raising the bias voltage above +10 increases the transistor cut-off bias that must be overcome by the previous driving transistor; therefore low-gain transistors fail. Lowering the bias voltage below +10 reduces transistor base bias and noise rejection and thus provides a test to detect high-leakage transistors and to simulate high temperature conditions (to check for thermal runaway). Raising and lowering the -15 volt supply has little effect upon the logic circuits, since it is the collector load voltage which is clamped at -3 volts in most modules. It does, however, increase and decrease the output pulse amplitude of pulse amplifier circuits (such as in delay modules) and so provides a check of the sensitivity of circuits which follow.

By recording the level of bias voltage at which circuits fail, progressive deterioration can be plotted and expected failure dates predicted. Therefore, these checks provide a means of planned replacement. Varying the +10 A supply to module mounting panel 2A changes the slice level of all of the Type 1537 Drum Sense Amplifier modules. Therefore, the margins give a good indication of drum read capability. A positive margin can be used to locate the lowest output signal which can be read, and a negative margin can be used to detect the presence of a high noise level or low noise rejection level of a module. Failure to obtain a reasonable margin when lowering the +10 A supply indicates that the slice level is too low and the amplifier is not rejecting noise or that noise is being picked up as a data signal. A margin of ±3 volts should be obtained on the +10 A line in mounting panel 2A. A margin of ±2.5 volts should be attainable on the +10 B mounting panel in location 1C. All other mounting panels should be able to operate properly with both +10 A and +10 B lines biased ±4.0 volts. The -15 volt margin should be approximately +3 and -5 volts. It is important that the +10 volt A and B lines

should not be biased more than ±4 volts (especially on panels 1C and 1D containing the field select circuits) and the -15 volt supply line not be increased above -18 volts or damage can result within the logic.

Refer to the Power Supply and Distribution discussion in Section 2 for an explanation of the color-coded connector at the right side of each module mounting panel and for the function of the normal/marginal-check switches at the end of each panel. During marginal checking, operating voltages for a mounting panel are supplied to the color-coded connector from either the computer marginal check panel or from a separate supply and are selected by means of the toggle switches. To use the computer marginal check voltage to marginal check the parallel drums, set the +10MC/OFF/-15MC selector switch on the marginal check switch panel to the desired voltage, and adjust the potential to the nominal level of +10 or -15 vdc as indicated on the MARGINAL CHECK voltmeter on the computer marginal-check supply (Type 734 Variable Power Supply). To supply the marginal check voltage from a separate external power supply, connect the +10 output between the green (+) and black (-) color-coded connector and connect the -15 vdc marginal check supply between the yellow (-) and black (+) color-coded connectors. To mate with the color-coded connector, the power supply outputs should be provided with a spade-lug, such as an AMP 42025-1 Power Connector. Terminals of the color-coded connectors on each mounting panel are wired in common so that the external supply need be connected only once to check all supplies. Selection of the normal internal power supply or the external marginal-check power supply is accomplished by means of the three normal/marginal-check toggle switches on each mounting panel. These switches select the source (normal internal or marginal external) of the service voltage supplied to terminals A, B, and C, respectively, of all modules in a panel.

To perform the check:

1. Assure that all of the normal/marginal-check switches on all panels of the parallel drum are in the down position; then connect the external marginal supply (or supplies) to the color-coded connector from either the computer or a separate external supply as described previously.

2. Energize the external marginal-check power supply and adjust its outputs to supply the nominal +10 vdc and -15 vdc.

3 Set the top normal/marginal sheet switch on the mounting panel to be checked to the up position.

4. Start operation of the parallel drum in a repetitive program or in a routine which fully utilizes the circuits in the mounting panel to be tested. The diagnostic program described in Appendix 1 is excellent for this check.

5. Lower the +10 volt marginal-check power supply output in small increments until normal parallel drum operation is halted. Record the marginal-check voltage. At this point marginal transistors can be located and replaced if desired. Return the marginal-check power supply output to the nominal +10 vdc level.

6. Restart operation of the parallel drum program. Then decrease the +10 volt marginal-check supply output until the parallel drum program halts again. Again, marginal transistors can be located and replaced. Record the marginal check voltage and return the bias voltage to the nominal +10 vdc level.

7. Return the top normal/marginal-check switch to the down position.

8. Repeat steps 2 through 7 for the center normal/marginal-check switch on the mounting panel being checked.

9. Repeat steps 2 through 8 for each mounting panel to be checked for positive and negative margins on the +10 vdc line. If the -15 vdc service lines are to be marginal tested, proceed to step 10, if not proceed to step 11.

10. Set the bottom normal/marginal-check switch to the up position, restart the program, and adjust the -15 vdc external marginal-check supply output until the parallel drum program is halted. Perform this operation to bias the -15 vdc line first positive and then negative, recording the levels attained in each direction. Return the lower normal/marginal-check switch to the down position. Repeat this step for each mounting panel to be checked for -15 vdc margins.

11. De-energize and disconnect the external marginal-check power supplies.

CORRECTIVE MAINTENANCE

The Type 23 Parallel Drum system is constructed of highly reliable transistorized modules and standard circuits. Use of these circuits and faithful performance of the preventive maintenance tasks ensure relatively little equipment down time due to failure. Should a malfunction occur, the condition should be analyzed and corrected as indicated in the following procedures. No special tools or test equipment are required for corrective maintenance other than a broad bandwidth oscilloscope and a standard multimeter. The best corrective maintenance tool is a thorough understanding of the physical and electrical characteristics of the system. Persons responsible for maintenance should become thoroughly familiar with the system concept as described in Section 2, specific circuit modules as described in Appendix 2 and the Digital Modules Catalog, the engineering drawings presented in Appendix 3, and the location of mechanical and electrical components as described in Section 1 and in the beginning of this section.

Diagnosis and remedial action for a fault condition are performed in the following phases:

a. Preliminary investigation to gather all information and to determine the physical and electrical security of the drum system.

b. System troubleshooting to locate the fault to within a module through the use of diagnostic programming, signal tracing, or aggravation techniques.

c. Circuit troubleshooting to locate defective parts within a module.

d. Repairs to replace or correct the cause of a malfunction.

e. Validation test to assure that the fault has been corrected.

f. Log entry to record pertinent data.

Preliminary Investigation

It is virtually impossible to outline any specific procedures for locating faults within a complexed digital system such as the parallel drum. Before commencing troubleshooting procedures, explore every possible source of information. Ascertain all possible information concerning any unusual function of the system prior to the fault and all possible program information such as routine in progress, condition of indicators, etc. Search the maintenance log to determine

if this type of fault has occurred before or if there is any cyclic history of this kind of fault, and determine how this condition was previously corrected. When the entire drum system fails, perform a visual inspection to determine the physical and electrical security of all power sources, cables, connectors, etc. Assure that the power supplies are working properly and that there are no power short circuits by performing the Power Supply Checks as described under Preventive Maintenance.

System Troubleshooting

Do not attempt to troubleshoot the parallel drum system without first gathering all information possible concerning the fault, as outlined under Preliminary Investigation.

Commence troubleshooting by performing that operation in which the malfunction was initially observed, using the same program. Thoroughly check the program for proper control settings, and note all indicator light operations before and at the time of the error. Careful checks should be made to assure that the drum system is actually at fault before continuing with corrective maintenance procedures. Loose or faulty cable connections can give indications very similar to those caused by drum malfunction. Faulty ground connections between pieces of equipment are a common source of trouble. From the portion of the program being performed and the general condition of the controls and indicators, a logical section of the machine at fault can usually be determined if the parallel drum is not functioning properly.

If the fault has been determined to lie within the Type 23 Parallel Drum, but cannot be localized to a specific logic function, perform the diagnostic program procedure. When the location of the fault has been narrowed to a logic element, continue troubleshooting to locate the defective module or component by means of signal tracing. If the fault is intermittent, a form of aggravation tests should be employed to locate the source of the fault.

Diagnostic Program

The most efficient means of troubleshooting the parallel drum makes use of the parallel drum diagnostic program tape described in Appendix 1. This routine provides a test of the reading, writing, or exchange operations of the parallel drum. Use of this program, combined with the Marginal Checks procedures described under Preventive Maintenance, provides a complete test of the data transfer operations of the parallel drum.

A valuable test of playback voltages from the read/write heads can be obtained when running the diagnostic program. Observe the outputs of the various read/write heads at terminal S of the appropriate Type 1537 Drum Sense Amplifier module. The output at this terminal provides a means of monitoring the actual output voltage of the read/head as amplified approximately 30-to-33 times. This output voltage at terminal S should appear as a peak-to-peak voltage of between 1.4 and 2.0 volts during a read operation. Any large descrepancies from this voltage indicate that a minor adjustment of the read/head is required as described under Data Head Spacing Checks described under Preventive Maintenance.

Another valuable test of playback voltages from the read/write heads can be obtained by running the diagnostic program and performing a marginal check of the +10 A voltage supplied to mounting panel 2A. This test varies the slice level of the Type 1537 Drum Sense Amplifier modules. If the program runs error free with margins of ±3 volts, no head adjustment should be attempted. Failure to obtain a margin of ±3 volts indicates that the heads are not adjusted properly or slice level may be too low, the sense amplifier is not rejecting noise, and the noise is being picked up as a data signal. Under these conditions perform the Drum Sense Amplifier checks specified under Preventive Maintenance.

Signal Tracing

If the fault has been located within a functional logic element, program the parallel drum to repeat some operation in which all functions of that logic element are utilized. If this test is to be performed without the use of the computer, control flip-flops or register flip-flops can be cleared or set manually by momentarily supplying a ground potential to the appropriate flip-flop output terminals. Counting operations of registers can be checked by supplying count pulses to the register from the output of the variable clock at location 1F2F and enabling the clock by supplying a ground connection to terminal 1F2V. If this output is too fast (every 2 to 5 microseconds), slower count pulses can be obtained from the clock signal at terminal 2B4E (every 8.5 microseconds) or from the index pulse at location 2B3E (every 35 milliseconds). Under these conditions, use the oscilloscope to trace signal flow through the suspected logic element. Oscilloscope sweep may be synchronized with any drum control signal by connecting the trigger input to the appropriate module terminal on the wiring side (front) of the equipment. The circuits most likely to encounter difficulty are those sending or receiving signals with the

PDP-1D or memory control. Trace output signals from the connector back to the origin, and trace input signals from the connector to its final destination. The signal tracing method can be used to determine with absolute certainty the quality of pulse amplitude, duration, and rise time and the correct timing sequence of this signal. If an intermittent malfunction occurs, signal tracing must be combined with an appropriate form of aggravation test.

There are four recorded index tracks and four recorded clock tracks. In the event any presently implemented index or clock tracks become destroyed, change the sense amplifier input wires from the presently implemented read/head to one of the spare heads. Read/write heads 0 through 3 of the pad at location H6 are recorded with an index mark, and heads 4 through 7 at position H6 are recorded with the 4096-bit clock track information.

Aggravation Tests

Intermittent faults should be traced through aggravation techniques. Intermittent logic malfunctions are located by performance of the marginal-check procedures as described under Preventive Maintenance. If this procedure locates the fault to within a specific module, marginal checking of that specific module alone can be performed as described under Circuit Troubleshooting.

Intermittent failures caused by poor wiring connections can often be revealed by vibrating the modules while running a repetitive routine, such as the diagnostic program. Often, wiping the handle of a screwdriver across the back of a suspect row of modules is a useful technique. By repeatedly starting the program and vibrating fewer and fewer modules, the malfunction can be localized to within one or two modules. After isolating the malfunction in this manner, check the seating of the modules in the connector, check the module connector for wear and misalignment, and check the module wiring for cold solder joints or wiring kinks.

Circuit Troubleshooting

The procedure followed for troubleshooting and correcting the cause of faults within modules and power supplies depends upon the down time limitations of parallel drum use. Where down time must be kept at a minimum, it is suggested that a provisioning parts program be adopted to maintain one spare module or power supply which can be inserted into the cabinet when System Troubleshooting procedures have traced the fault to a particular component. A list of

modules and power supplies can be compiled from the list of drawings presented in Appendix 3 of this manual. Component troubleshooting procedures can be performed within the equipment as in-line dynamic tests or can be performed at a bench as either static or dynamic tests.

Module Circuits

Circuit schematics of each module are supplied in Appendix 3 of this manual and should be referred to for detailed circuit information. The basic functions and specifications for standard modules are presented in the Digital Modules Catalog, A-705, and the functions of modules peculiar to drum systems are described in Appendix 2. The following design considerations may also be helpful in troubleshooting standard DEC modules.

a. Forward-biased silicon diodes are used in the same manner as zener diodes, usually to provide a voltage differential of 0.75 volts. For instance, a series string of four diodes is used to produce the -3 vdc clamp voltage used in most modules.

b. The state of DEC flip-flops is changed by an incoming pulse which turns off the conducting transistor amplifier. Since flip-flops use PNP transistors, the input pulse must be positive and must be coupled to the base of the transistor. Flip-flop modules that accept negative pulses to change the state invert this pulse by means of a normal transistor inverter circuit.

c. Each Type 1304 and Type 4301 Delay module consists of an input buffer amplifier which is transformer-coupled to a monostable multivibrator. The multivibrator output is directly coupled to a level amplifier and transformer-coupled to an output pulse amplifier.

d. The Type 4604 Pulse Amplifier module contains three independent circuits, each containing a monostable multivibrator and an output pulse amplifier. The period of the monostable multivibrator is determined by an RC time constant which is determined by external connections to the module. The output from the pulse amplifier is determined by the period of the monostable multivibrator and therefore ranges between 0.4 and 1 microsecond.

e. The Type 1607 Pulse Amplifier module contains three independent pulse amplifiers, each with its own input gating inverter. Output pulse duration is determined by the time required to saturate the interstage coupling transformer. No multivibrators or other RC timing circuits are used in this pulse amplifier.

f. The Type 4519 Drum Field Select module is a 3-state device which places a field of read/write heads in either the read, write, or deselected condition. In the read state the module serves as a 20 milliampere current source for the read/write heads. In the deselected state the module provides a +0.5 volt bias for the head selection diode matrix. In the write state the module output is at -14 volts and accepte currents from the Type 4518 Drum NRZ Writer. These three conditions may be observed at terminal W. This circuit uses silicon control rectifiers to place the output terminal at -14 volts and accept 1.75 amperes of write current. With elevated temperatures, it is possible for the silicon controlled rectifiers to be turned on during a write state and unable to be deselected after the state has passed. This condition may be observed by running the diagnostic program, and stopping the program to monitor the output at terminal W with a voltmeter. An error is indicated if any output terminal is found at -14 volts which is not selected for the write state, as indicated by the contents of the write field buffer. This condition also causes the preamplifier output voltage at terminal S of the Type 1537 Drum Sense Amplifier modules to be considerably less than the normal 1.4 to 2.0 volt peak-to-peak signal.

In-Line Dynamic Tests

Where down time is not critical, the spare parts list can be reduced and signal tracing techniques can be utilized to troubleshoot modules within the buffer. This practice involves module removal by means of a Type 1906 System Module Puller, insertion of a Type 1954 System Module Extender into the logic panel, insertion of the suspect module in the module extender, and oscilloscope signal tracing of the module with the equipment operating in some test routine which exercises the module.

In-Line Marginal Tests

Marginal checks of individual modules can be performed within the parallel drum to test specific modules of questionable reliability, or to further localize the cause of an intermittent failure which has been localized to within one module by the normal marginal checking method. These checks are performed with the aid of a modified Type 1954 System Module Extender. To modify an extender for these checks, disconnect the small wire leads from terminals A, B, and C of the connector block, and solder a 3-foot test lead to each of the three wires. Attach a spade lug, such as an AMP 42025-1 Power Connector to the end of each test lead, and label each to correspond to the A, B, or C terminal from which the wire was disconnected. To marginal check a module within the parallel drum:

1. De-energize the parallel drum.

2. Remove the module to be checked from the module mounting panel, replace it with the modified extender, and insert the module in the extender.

3. Connect test leads A, B, and C to the appropriate terminals of the color-coded connector at the end of the mounting panel. The module being checked can then draw power from the external marginal-check power supply via the green (+10 vdc) or yellow (-15 vdc) terminals, or from the normal internal power supplies via the red (+10 vdc) or blue (-15 vdc) terminals. Note that the normal/marginal-check switches at the end of the mounting panel should remain in the down position during the entire procedure.

4. Restore machine power, adjust the marginal-check power supply to provide nominal voltage outputs, and start operation of a routine which fully utilizes the module being checked.

5. Increase or decrease the output of the marginal-check power supply until the routine stops, indicating module failure. Record each bias voltage at which the module fails. Also record the condition of all operator console controls and indicators when a failure occurs. This information indicates the module input conditions at the time of failure and is often essential to tracing the cause of a fault to a particular component.

6. Repeat steps 1 and 3 through 5 for each of the three bias voltages. If margins of ±4 volts on the ±10 vdc supplies, and +3 and -5 volts on the -15 vdc supplies can be obtained without adversely affecting the logic function of the module, it can be assumed to be operating satisfactorily. If the module fails before these margins are obtained, use normal signal tracing techniques within the module to locate the source of the fault.

If a dual-voltage variable power supply is available, perform steps 1 and 2; connect test leads A, B, and C to either the normal machine power supplies at the red (+10 vdc) and blue (-15 vdc) terminals at the end of the module panel or directly to output at this supply; then continue the procedure from step 4. When using this connector, the ground connectors of the dual-voltage supply must be connected to buffer signal ground. This connection can be made to the black connector at the end of either module mounting panel.

Static Bench Tests

Visually inspect the module on both the component side and the printed-wiring side to check for short circuits in the etched wiring and for damaged components. If this inspection fails to reveal the cause of trouble or to confirm a fault condition observed, use the multimeter to measure resistances.

CAUTION

Do not use the lowest or highest resistance ranges of the multimeter when checking semiconductor devices. The X10 range is suggested. Failure to heed this warning may result in damage to components.

Measure the forward and reverse resistances of diodes. Diodes should measure approximately 20 ohms forward and more than 1000 ohms reverse. If readings in each direction are the same, and no parallel paths exist, replace the diodes.

Measure the emitter-collector and emitter-base resistances of transistors. Most catastrophic failures are caused by short circuits between the collector and the emitter or are caused by an open circuit in the base-emitter path. A good transistor indicates an open circuit in both

directions between collector and emitter. Normally 50 to 100 ohms exist between the emitter and base or between the collector and the base in the forward direction, and open-circuit conditions exist in the reverse direction. To determine forward and reverse directions a transistor can be considered as two diodes connected back-to-back. In this analogy PNP transistors are considered to have both cathodes connected together to form the base, and both the emitter and collector assume the function of an anode. In NPN transistors the base is assumed to be a common-anode connection, and both the emitter and collector are assumed to be the cathode.

Multimeter polarity must be checked before measuring resistances, since many meters (including the Triplett 630) apply a positive voltage to the common lead in the resistance mode. Note that although incorrect resistance readings are a sure indication that a transistor is defective, correct readings give no guarantee that the transistor is functioning properly. A more reliable indication of diode or transistor malfunction is obtained by using one of the many inexpensive in-circuit testers commercially available.

Damaged or cold-solder connections can also be located using the multimeter. Set the multimeter to the lowest resistance range and connect it across the suspected connection. Poke at the wires or components around the connection, or alternately rap the module lightly on a wooden surface, and observe the multimeter for open-circuit indications.

Often the response time of the multimeter is too slow to detect the rapid transients produced by the intermittent connections. Current interruptions of very short durations, caused by an intermittent connection, can be detected by connecting a 1.5-volt flashlight battery in series with a 1500-ohm resistor across the suspected connection. Observe the voltage across the 1500-ohm resistor with an oscilloscope while probing the connection.

Dynamic Bench Tests

Dynamic bench testing of modules can be performed through the use of special equipment. A Type 922 Test Power Cable and either a Type 722 or Type 765 Power Supply can be used to energize a system module. These supplies provide both the +10 vdc and -15 vdc operating power for the module as well as ground and -3 volt sources which may be used to simulate signal inputs. The signal input potentials can be connected to any terminal normally wired to receive logic level signals by means of eyelets provided on the power cable. Type 911 Patch Cords may be used to make these connections between eyelets on the plug. In this manner logic operations and voltage measurements can be made throughout the circuit. When using the Type 765 Bench Power Supply, marginal checks of an individual module can also be obtained.

Repair

In all soldering and unsoldering operations in the repair and replacement of parts, avoid placing excessive solder or flux on adjacent parts or service lines. When soldering semiconductor devices (transistors, crystal diodes, and metallic rectifiers) which may be damaged by heat, the following special precautions should be taken:

a. Use a heat sink, such as a pair of pliers, to grip the lead between the device and the joint being soldered.

b. Use a 6-volt soldering iron with an isolation transformer. Use the smallest soldering iron adequate for the work.

c. Perform the soldering operation in the shortest possible time to prevent damage to the component and delamination of the module etched wiring.

When any part of the equipment is removed for repair and replacement, make sure that all leads or wires which are unsoldered, or otherwise disconnected, are legibly tagged or marked for identification with their respective terminals. Replace defective comments only with parts of equal or greater quality or narrower tolerance.

When replacing a Type 4518 Drum NRZ Writer, remove the two wire jumpers near the center of the component side of the printed wiring board. This operation disconnects 1000 picofarad capacitors C4 and C5 from the circuit and prevents their shunting the output to ground.

Validation Test

Following the replacement of any electrical component in the equipment, a test should be performed to assure the correction of the fault condition and to make any adjustment of the timing or signal levels affected by the replacement. This test should be taken from the Preventive Maintenance procedure most applicable to the portion of the system in which the fault was found. For example, if a filter capacitor was replaced in one of the power supplies, the ripple check for that power supply should be repeated as specified under Power Supply Checks. Or, if a delay module is repaired or replaced, the Timing Checks should be repeated. If repairs or replacement are made in an area which is not checked on preventive maintenance, an appropriate operational test should be devised. Normally the diagnostic program serves this purpose if the error was found in a logic element pertaining to data transfer functions. If the

fault occurred in the addressing or control elements of the machine, such as a flip-flop replacement, the register or control function performed by the flip-flop should be completely checked by manually setting and clearing or by programmed exercise of that function.

When time permits, it is suggested that the entire preventive maintenance tasks be performed as a validation test. The reasons for this are:

a. If one fault occurred and was corrected, other components may be marginal.

b. While the equipment is down and available, preventive maintenance can be performed and need not be scheduled again for four months (or the normal period).

Log Entry

Corrective maintenance activities are not completed until they are recorded in the maintenance log. Record all data indicating the symptoms given by the fault, the method of fault detection, the component at fault, the results of the validation tests, and any other information which would be helpful in maintaining the equipment in the future.

APPENDIX 1

TYPE 23 PARALLEL DRUM DIAGNOSTIC PROGRAM

This program is designed as a diagnostic test of the Type 23 Parallel Drum, and can be obtained from the DEC Program Library as symbolic tape DEC-1-137-M*. The program uses the computer switches as outlined in Table A1-1.

TABLE A1-1 DIAGNOSTIC PROGRAM SWITCH USAGE

Switch	Function
Test Word 0-5	Select core bank for drum data (bank "0" not valid)
Sense Switch 1	Rejects errors
Test Address = 100	Starting address for full test
Test Address = 101	Data list, 4096 words
Test Address = 102	16 channel break system used

The program employs error stops and error printouts in checking the drum. All error stops ask the question, "Is a core band selected?" Data errors are printed in the following format: memory address, correct word, error word (in red), read field, drum word count. For example, (PAR RD WR X) means a parity error occurred during a drum data exchange, with X indicating the contents of the DCL when the error was detected. Table A1-2 lists the error printouts and causes.

TABLE A1-2 ERROR PRINTOUTS

Printout	Cause
DRA	The DRA instruction failed.
DBA	No sequence break. Instruction DBA or sequence break system failed.

*The program as described in this appendix was accurate at the time of publication. However, programs in the library are continually being revised, so periodic checks should be made to assure that the most recent program is used in a diagnostic test.

TABLE A1-2 ERROR PRINTOUTS (continued)

Printout	Cause
PAR	Parity error
TIM	Timing error
RD	Reading error
WR	Writing error

Figures A1-1, A1-2, and A1-3 are three flow charts which diagram the test. A program listing for the entire test follows the flow charts.

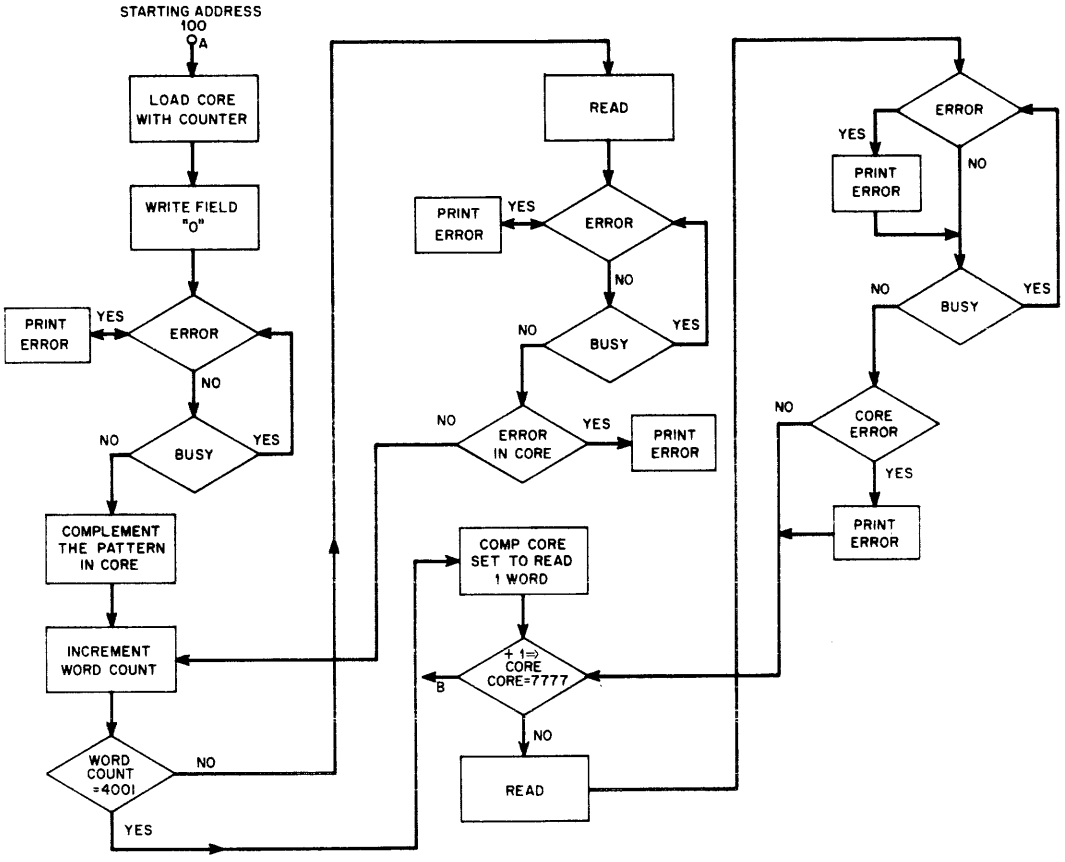


Figure A1-1 Parallel Drum Type 23 Test

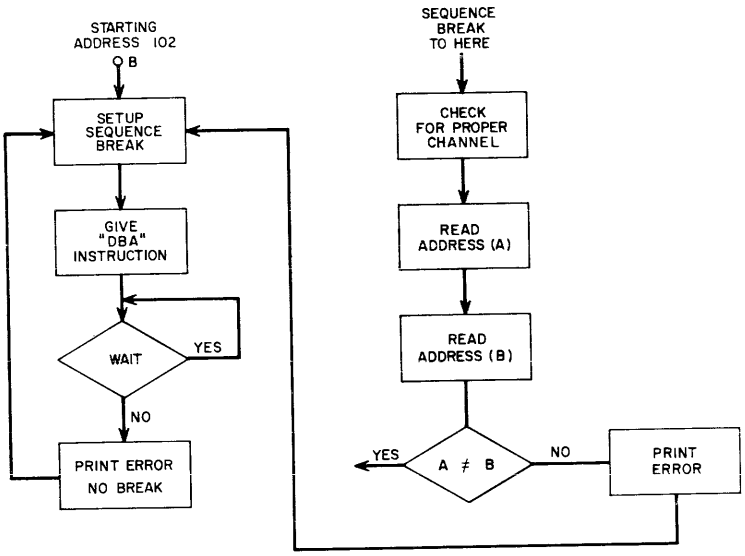


Figure A1-2 Sequence Break

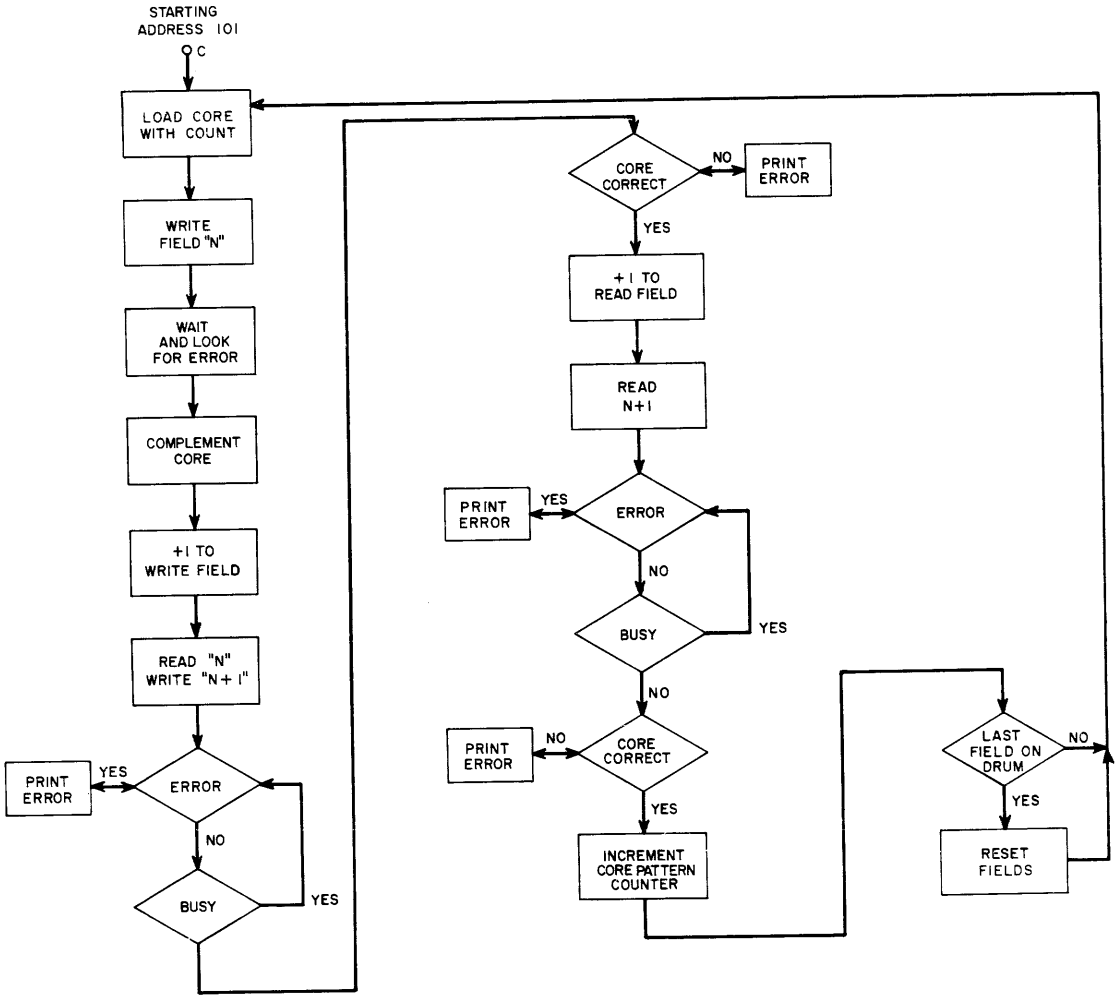


Figure A1-3 4096 Word Transfer Starting with Field Zero

```
/ drum
            eem=724074
            dzm t4
            dzm c1
            dzm cnt
            dzm i1
            dzm wc

            dia=720061
            dba=722061
            dwc=720062
            dcl=720063
            dra=722062

define      busy A
            cks
            rir 1
            spi
            jmp A
            term

define      bank
            lat
            and (770000
            sza i
            hlt
            dac cl
            term

define      update A
            lac A
            add (1001
            dac A
            term

define      error
            dra
            dio t4
            spi
            jsp err
            term

define      space
            cli
            tyo
            term

define      return
            lio (77
            tyo
            term
```

```
define      typred
            lio (35
            tyo
            term

define      black
            lio (34
            tyo
            term

define      movec A,B
            lac A
            and (7777
            sza i
            ior (10000
            cma
            dac B
            term

define      fieldr
            lac il
            add (10000
            dac il
            term

define      fieldw
            lac wc
            add (10000
            dac wc
            term



/drum -1

100/        jmp ll
            jmp sta
stc,        iot 56      /clear break system
            iot 55      /enter seq mode
            iot 53      /clear channels
            iot 551
            iot 4074    /set ext mode


            dzm tem     /store jsp in break
            lio (jsp sc2
            dio i tem
            idx tem
            sas (100
            jmp .-3
```

```
sc1,        dzm tem
            load t2,700000
            lio tem
            dba
            count t2,.
            iot 54
            lac (flexo dba      /no seq break
            return
            jda tya
            jmp stc

sc2,        iot 54
            and (7777
            sad (30
            jmp sc3
            dac t4    /seq to wrong channel
            lac (flexo seq
            return
            jda tya
            space

            law i 3
            add t4
            and (77
            jda opt   /print pc storage
            jmp stc

sc3,        iot 56
            dra
            dio t4
            dra
            swap
            sas t4    /ok if diffirent
            jmp sta

            return
            lac (flexo dra
            jda tya
            jmp stc   /dra failed


sta,        724074    /enter extend mode
            dzm tem
            dzm t2
            dzm t3

            cla -opr clf 7
            dac il
            bank
            dzm wc
            dzm cnt   /initialize program
```

```
st1,        jsp cou    /load core with counter
            stf 6
            jsp drm    /write

st2,        error
            busy st2
            jsp com    /complement pattern
            fieldw
            stf 5
            jsp drm    /read n, write n+1

st3,        error
            busy st3
            clf 7
            jsp chk    /check core for count

            stf 5
            fieldr
            stf 4
            jsp drm    /read n+1
foo,        error
            busy foo
            jsp chk    /check comp count
            update cnt
            clf 7

st4,        law i 7777
            and il
            sas (370000
            jmp st1
            cla
            dip wc
            dip il
            jmp st1




il,         724074
            clf 7
            dzm cnt
            dzm wc
            dzm il
            bank
            jsp cou    /load core with count

            stf 6
            jsp drm    /write core
```

```
xk1,        error
            busy xk1
            jsp com     /comp core
            clf 6       /clear write
            stf 5       /set read

xk3,        idx wc      /inc word count
            sad (4001
            jmp xk4

            jsp drm     /read
xk2,        error
            busy xk2
            jsp chk     /check for errors
            jmp xk3

xk4,        dzm il      /test core location
            law 1
            dac wc
            jsp com     /comp core
xk6,        idx cl
            and (7777
            sad (7777           /test for last
            jmp stc

            jsp drm     /read 1 word
xk5,        error
            busy xk5

            lac cnt
            sad i cnt           /test for error
            jmp xk6

            lac (flexo cl
            return
            jda tya
            lac cl
            jda opt
            jmp xk6     /core error

drm,        dap dr      /drum subroutine
            busy drm 1
            lac il
            szf 5
            ior (400000
            swap
            dia         /drum initial address

            lac wc
            szf 6       /set for write
            ior (400000
```

```
            swap
            dwc         /drum word count
            lio cl
            dcl
dr,         jmp .

com,        dap cm2   /complement core
            movec wc,tem
            move cl,t2
cm1,        lac i t2
            cma
            dac i t2
            idx t2
            count tem,cm1
cm2,        jmp .

chk,        dap ck2   /check core
            movec wc,tem
                      move cl,t2
            move cnt,t3

ck1,        lac i t2
            szf 4
            cma
            sas t3
            jsp er    /error routine
            idx t2
            update t3
            count tem,ck1
            law 7777
            and wc
            sza i
            jmp ck2
            lac i t2
            szf 4
            cma
            sas t3
ck2,        jmp .
            lac (flexo wce
            jda tya
            return
            jmp ck2

cou,        dap cu2   /core counter
            movec wc,tem
            move cl,t2
            move cnt,t3
cu,         lac t3
            dac i t2
            idx t2
            update t3
            count tem,cu
cu2,        jmp .
```

```
tya,        0          /type alpha
            dap ta
            lac tya
            repeat 3,rcl 77      tyo
            space
ta,         jmp .



err,        dap er2    /error printer
            szs 10
            jmp er2    /reject errors
            return

            lio t4
            ril 1
            lac (flexo par
            spi
            jda tya    /print par

            lio t4
            ril 3
            lac (flexo tim
            spi
            jda tya    /print tim

            lac (flexo rd
            szf 5
            jda tya
            lac (flexo wr
            szf 6
            jda tya    /print read,write

            lac t4
            and (77777
            jda opt
er2,        jmp .      /print drum counter , exit

er,         dap ee     /data error printer
            szs 10
            jmp ee
            return
            lac t2
            jda opt    /print mem address
            space
```

```
        lac t3
        szf 4
        cma
        jda opt    /print correct word
        space

        typred
        lac i t2
        jda opt    /print error word
        space
        black

        law i 7777
        and i1
        ral 77
        jda opt    /print field
        space

        lac wc
        jda opt
ee,     jmp .      /print word count
```

OCTAL PRINTOUT SUBROUTINE LISTING FOR

DIAGNOSTIC PROGRAM

```
/octal print subroutine -- revised 2 June 62

/unsigned, leading zero eliminating.  Call: number in ac, jda opt

opt,        0
            dap opx
            law i 6
            dac op2
            stf 1
op1,        szf i 1
opo,        tyo
            lio opt
            cla
            rcl 3s
            dio opt
            sza
            clf 1
            sza i
            law 20
            rcl 9s
            rcl 9s
            isp op2
            jmp op1
            xct opo
opx,        jmp .

op2,        0

constants
variables
start 11
```

APPENDIX 2

DRUM MODULES

The Type 23 Parallel Drum employs three types of standard DEC system modules which are unique to drum systems. These modules are described here in an effort to present all information pertinent to the parallel drum within one document.

TYPE 1537 DRUM SENSE AMPLIFIER

The Type 1537 module contains a preamplifier with a difference gain of 33, which produces linear amplification of drum head playback voltages of 30 millivolts peak-to-peak to an output voltage of 1 volt peak-to-peak. The preamplifier (Q1 through Q4) precedes a slicer (Q5, Q6, Q7) with a variable threshold; the output of the slicer is used as an enabling level for the pulse amplifier (Q8, Q9) contained in the module. When the input signal is of sufficient amplitude to produce a binary 1 output from the slicer, a strobe pulse at the input of the pulse amplifier produces a pulse at the output.

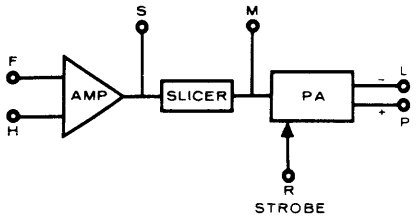


Figure A2-1
Type 1537 Logic Diagram

The Type 1537 is suitable for use with return-to-bias techniques within the pulse repetition frequency range of 50 kilocycles to 500 kilocycles.

Controls

A variable resistor controls the slice level, which may be adjusted from 0.1 to 0.4 volts at the output of the preamplifier. The preamplifier gain may be varied from 0 to 200 by substituting an appropriate value of resistance for the lug-mounted 300-ohm 1 per cent resistor. Gain is inversely proportionate to the value of this feedback resistor.

Input

The nominal input voltage for a selected magnetic head is 30 millivolts peak-to-peak. The

difference input impedance is approximately 1800 ohms. The common mode input impedance is approximately 480 ohms. Thus,if terminals H and F are connected through diodes to a drum head which has 1 milliampere bias current applied to its center tap, terminals H and F will rise to +4 volts from their quiescent +3.5 volt level. If the input voltage at terminal H is negative relative to that at terminal F, the circuit detects a binary 1.

The strobe is a DEC standard 70-nanosecond negative pulse. There must be a 200 microsecond settling time allowed from the selection of the magnetic head to the first strobe pulse.

Output

The output is a DEC standard 70-nanosecond pulse which occurs at the output every time the input signal meets the input requirement. Each output is capable of driving 16 units of pulse load.

Terminal M is at ground level when the input exceeds the slice level. The output at terminal M is capable of driving a DEC Type 1410 or 4410 Pulse Generator when an external 2200-ohm resistor is returned from terminal M to -15 volts. This function is useful in deriving clock pulses from a clock track.

Power

Sources of -15 volts/85 milliamperes, +10 volts (A)/0.2 milliamperes, and +10 volts (B)/20 milliamperes power are required for operation of this module.

TYPE 4518 DRUM NRZ WRITER

The Type 4518 module contains the circuit used to generate the write pulses in the read/write head of a magnetic drum. The circuit can supply a 100 milliampere pulse with a rise time between 0.50 and 0.75 microseconds to a center-tapped recording head of approximately 75 microhenries inductance. The circuit operates in the non-return to zero (NRZ) mode

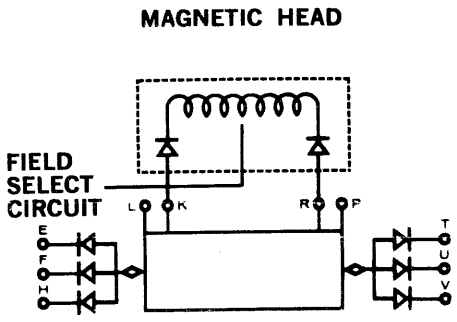


Figure A2-2
Type 4518 Logic Diagram

producing positive-going pulses from - 15 volts to ground. A 3-input ground-level AND gate controls the write pulse generating circuit.

Input

Signal inputs must be DEC standard levels or equivalent. The load is 1 unit of base load shared among the inputs with -3 volts on them. Each input must be at ground potential or disconnected to enable the gate and produce output current.

Output

Each output terminal (K and R) is grounded through 120 ohms when the input gate is properly enabled. When connected to a read/write head whose centertap is a nominal -14 volts, each output can supply approximately 100 milliamperes of writing current. When the input is disabled, the outputs are returned to -15 volts through 1500 ohms.

The rise time of the output pulse is variable from 0.50 to 0.75 microseconds. The module as shipped is set for the longer rise time, which minimizes noise in the writing pulse when both reading and writing occur simultaneously in a parallel drum system. An intermediate rise time can be obtained by connecting terminals K and L (and terminals P and R) together. This places a 4700 picofarad capacitor across the 120 ohm output resistor. The fastest rise time requires removing a jumper in each circuit, as well as connecting the output terminals together. This removes a 1000 picofarad capacitor from the output to ground.

Power

Operating power for the module is -15 volts/35 milliamperes, +10 volts (A)/0.16 milliamperes, and +10 volts (B)/5.2 milliamperes.

TYPE 4519 DRUM FIELD SELECT

The Type 4519 module contains a single drum field select circuit and two ground-level NAND gates. The drum field select circuit is a 3-state device that provides the mode selection bias for a group of parallel magnetic drum read/write heads. The two NAND gates are used to select one of the three stable states of the drum field select circuit.

As long as both NAND gates are disabled, the drum field select circuit is in the nonselected state. When the 2-input read select gate is enabled, the drum field select circuit is switched to the read select state and a disabling bias is applied to the write select gate. When the 3-input write select gate is enabled, the drum field select circuit is switched (after a 1 microsecond delay) to the write select state. The output of each NAND gate is available for monitoring the status of the gate or as a direct input of the drum field select circuit.

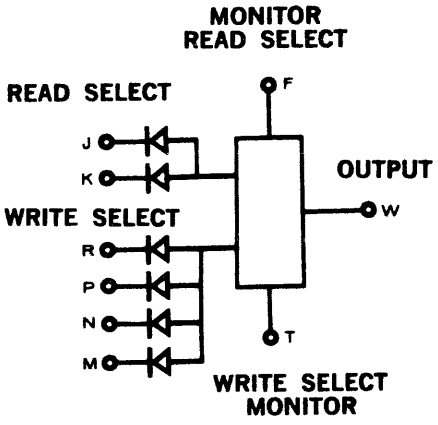


Figure A2-3
Type 4519 Logic Diagram

After the circuit has been switched to the read select state, 200 microseconds must be allowed to stabilize the reading current before the resulting information from the read/write heads is available. A reader or sense amplifier, such as the Type 1537, must be used to obtain the information from the read/write heads.

The 1 microsecond delay of the write select gate prevents the drum field select circuit from being immediately switched to the write select state. This delay allows the selecting circuits to completely settle into their enabling states. After the circuit is switched to the write select state, a minimum of 200 microseconds must be allowed before it can be changed to another state. After it is changed, a drop-out time of 100 microseconds must be allowed for.

Input

Input signals are DEC standard levels or equivalent. Each input must be at ground potential or disconnected to enable a gate. A single -3 volt level will disable a gate. The load is 1 unit of base load for each gate, shared among any negative inputs.

Output

The output can exist in one of the following three stable states:

Nonselected State — When neither NAND gate is enabled, a positive level of 1.0 volt (clamped by 7 milliamperes internally) is produced at the output, but no current flows in the select bus and the field of magnetic heads is not selected.

Read Select State — When the 2-input gate is enabled, the output terminal is at +4.0 volts and a positive current of 20 milliamperes flows from the output. This current is sufficient to connect a field of 20 read/write heads to the read bus, via their selection diodes. When less than 20 heads are used, the output must be loaded with a series resistor and diode to ground. The value of the resistor is

$$\frac{4000}{20-n} \text{ ohms,}$$

where n is the number of heads used.

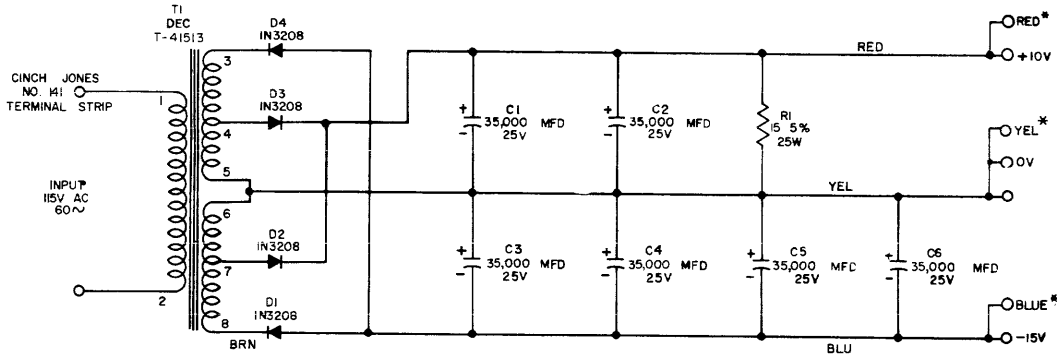
Write Select State — When the 3-input gate is enabled, the output terminal is at -14 volts and accepts a current of up to 2.0 amperes of write current from the read/write heads, via their selection diodes and write circuits (such as the Type 4518 module).

Power

The following power is required for operation of each module: -15 volts/2.0 amperes max, +10 volts (A)/0.16 milliamperes, +10 volts (B)/48 milliamperes.

APPENDIX 3

ENGINEERING DRAWINGS



* HEYMAN MFG. CO.
TAB TERMINALS

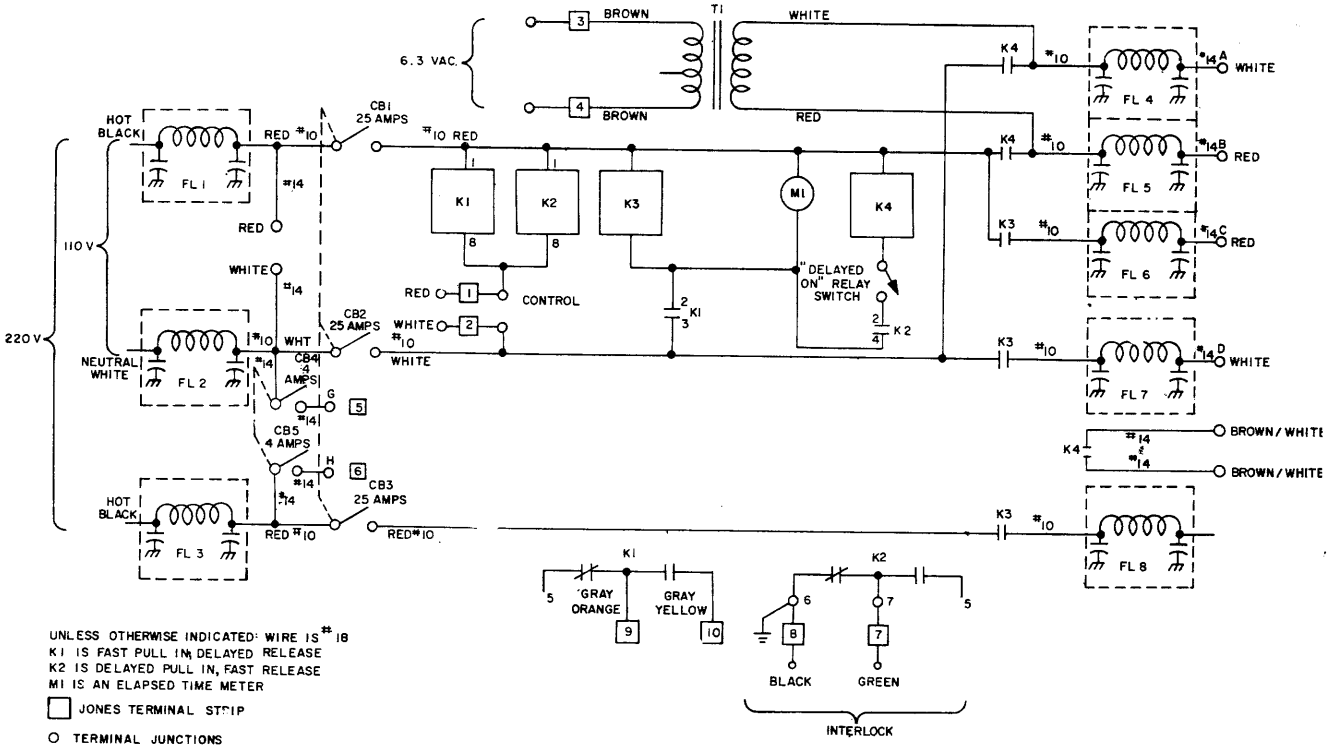
NOTE:
IN ORDER TO KEEP OUTPUT VOLTAGE WITHIN THE FOLLOWING LIMITS:
+10V: +9.5 TO +11V
-15V: -14.5 TO -16V
THE LOADING SHOULD BE WITHIN THE FOLLOWING LIMITS.

BOTH SIDES LOADED	+10 V	0 TO	7.0	AMPS
	-15 V	1.0 TO	8.0	AMPS
ONE SIDE LOADED	+10 V	0 TO	7.5	AMPS
	-15 V	1.0 TO	8.5	AMPS

SUM OF THE OUTPUT CURRENTS ARE LIMITED BY THE FOLLOWING EQUATION: $5I_{10} + 6I_{15} \leq 53$

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
IN3208	IN3208		

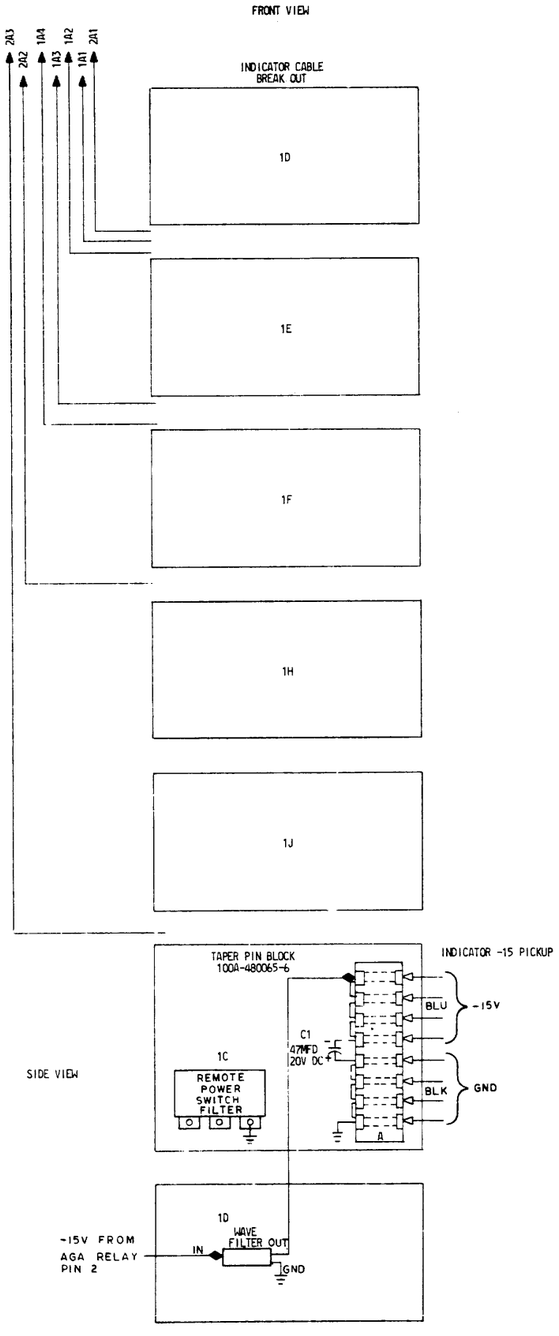
Power Supply RS-728

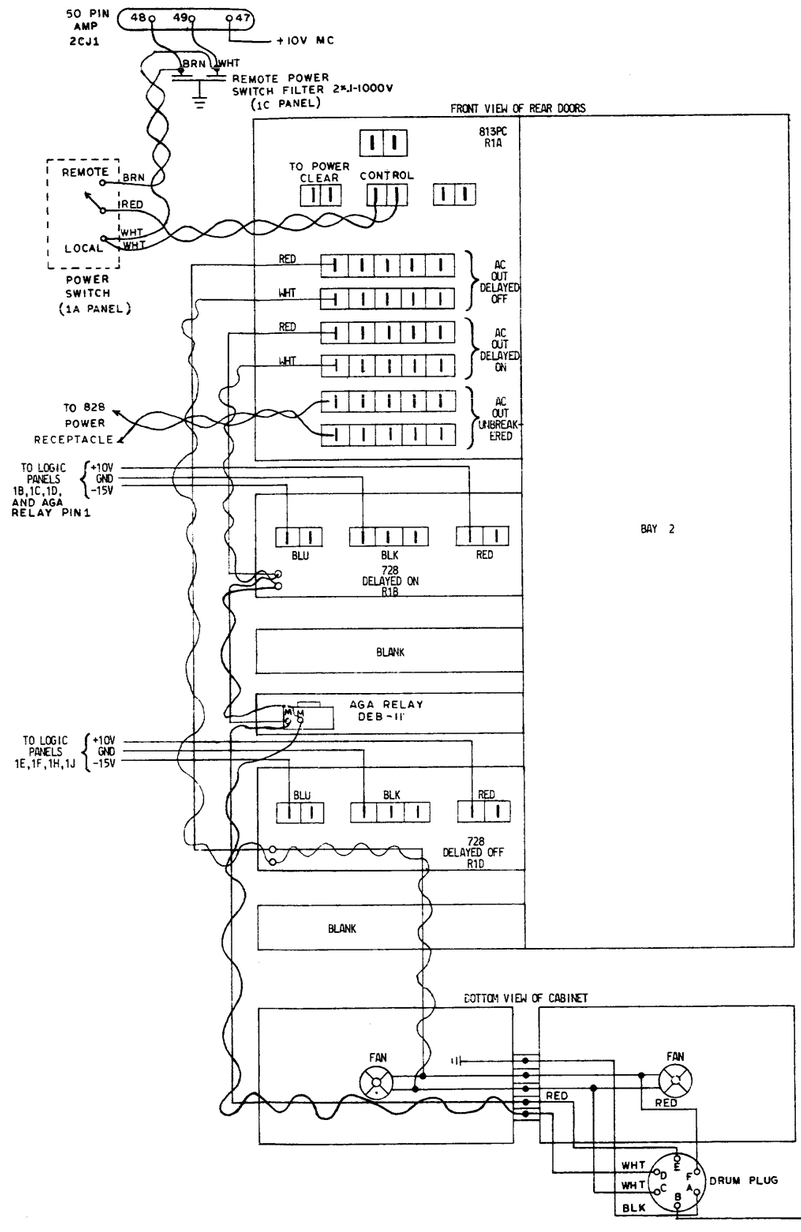


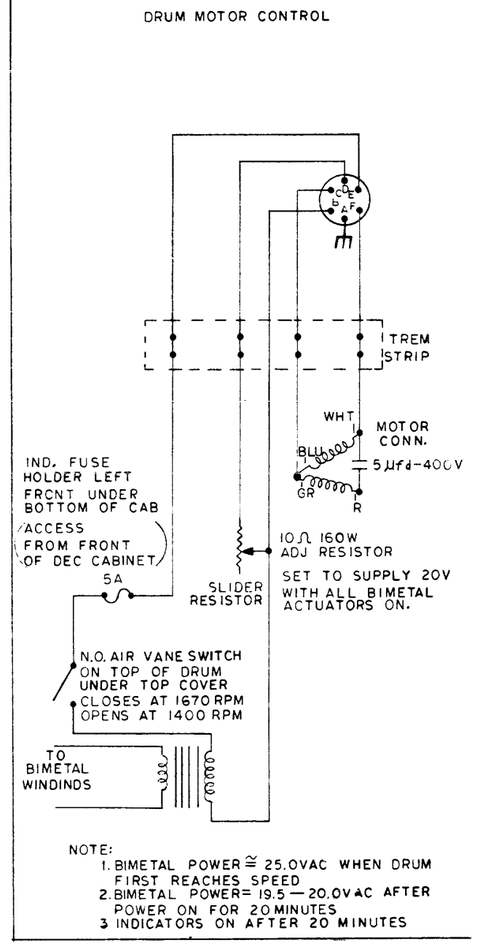
UNLESS OTHERWISE INDICATED: WIRE IS #18
K1 IS FAST PULL IN, DELAYED RELEASE
K2 IS DELAYED PULL IN, FAST RELEASE
M1 IS AN ELAPSED TIME METER
☐ JONES TERMINAL STRIP
○ TERMINAL JUNCTIONS

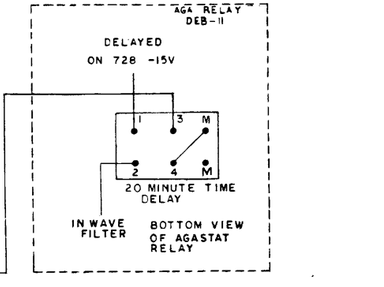
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA

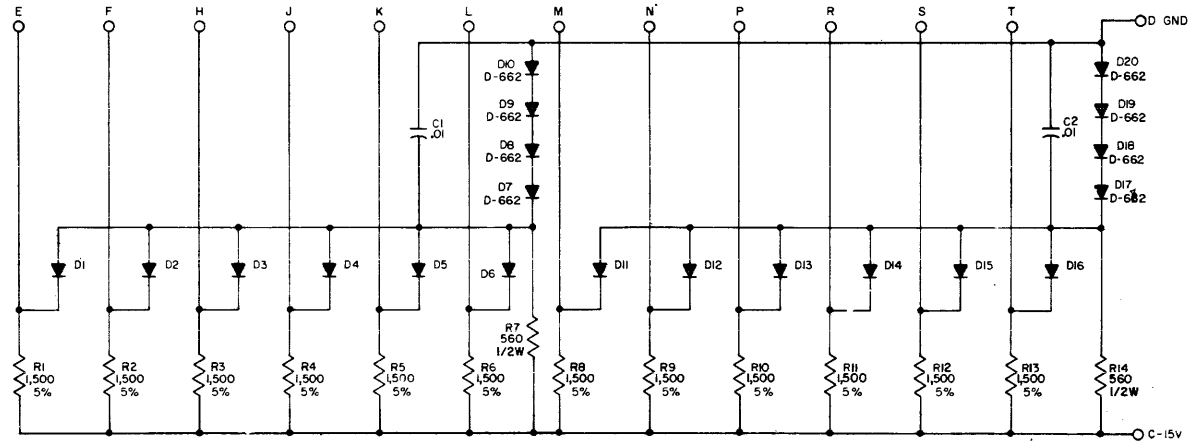
Power Control RS-813


FRONT VIEW
2A3
2A2
1A4
1A3
1A2
1A1
2A1
INDICATOR CABLE BREAK OUT
1D
1E
1F
1H
1J
TAPER PIN BLOCK 100A-480065-6
INDICATOR -15 PICKUP
BLU
-15V
GND
BLK
C1 47MFD 20V DC
1C
REMOTE POWER SWITCH FILTER
SIDE VIEW
1D
WAVE FILTER OUT
IN
GND
-15V FROM AGA RELAY PIN 2


50 PIN AMP 2CJ1
48
49
47
+10V MC
BRN
WHT
REMOTE POWER SWITCH FILTER 2*J-1000V (1C PANEL)
FRONT VIEW OF REAR DOORS
813PC R1A
TO POWER CLEAR
CONTROL
REMOTE
BRN
RED
WHT
LOCAL
WHT
POWER SWITCH (1A PANEL)
RED
WHT
AC OUT DELAYED OFF
RED
WHT
AC OUT DELAYED ON
AC OUT UNBREAK-ERED
TO 828 POWER RECEPTACLE
TO LOGIC PANELS 1B,1C,1D, AND AGA RELAY PIN1
+10V
GND
-15V
BLU
BLK
RED
728 DELAYED ON R1B
BAY 2
BLANK
AGA RELAY DEB-11
WHT
TO LOGIC PANELS 1E,1F,1H,1J
+10V
GND
-15V
BLU
BLK
RED
728 DELAYED OFF R1D
BLANK
BOTTOM VIEW OF CABINET
FAN
FAN
RED
RED
WHT
WHT
BLK
DRUM PLUG


DRUM MOTOR CONTROL
TREM STRIP
WHT
MOTOR CONN.
BLU
5 µfd-400V
GR
R
IND. FUSE HOLDER LEFT FRONT UNDER BOTTOM OF CAB
ACCESS FROM FRONT OF DEC CABINET
5A
10Ω 160W ADJ RESISTOR
SET TO SUPPLY 20V WITH ALL BIMETAL ACTUATORS ON.
SLIDER RESISTOR
N.O. AIR VANE SWITCH ON TOP OF DRUM UNDER TOP COVER
CLOSES AT 1670 RPM
OPENS AT 1400 RPM
TO BIMETAL WINDINDS
NOTE:
1. BIMETAL POWER ≅ 25.0VAC WHEN DRUM FIRST REACHES SPEED
2. BIMETAL POWER= 19.5 — 20.0VAC AFTER POWER ON FOR 20 MINUTES
3 INDICATORS ON AFTER 20 MINUTES

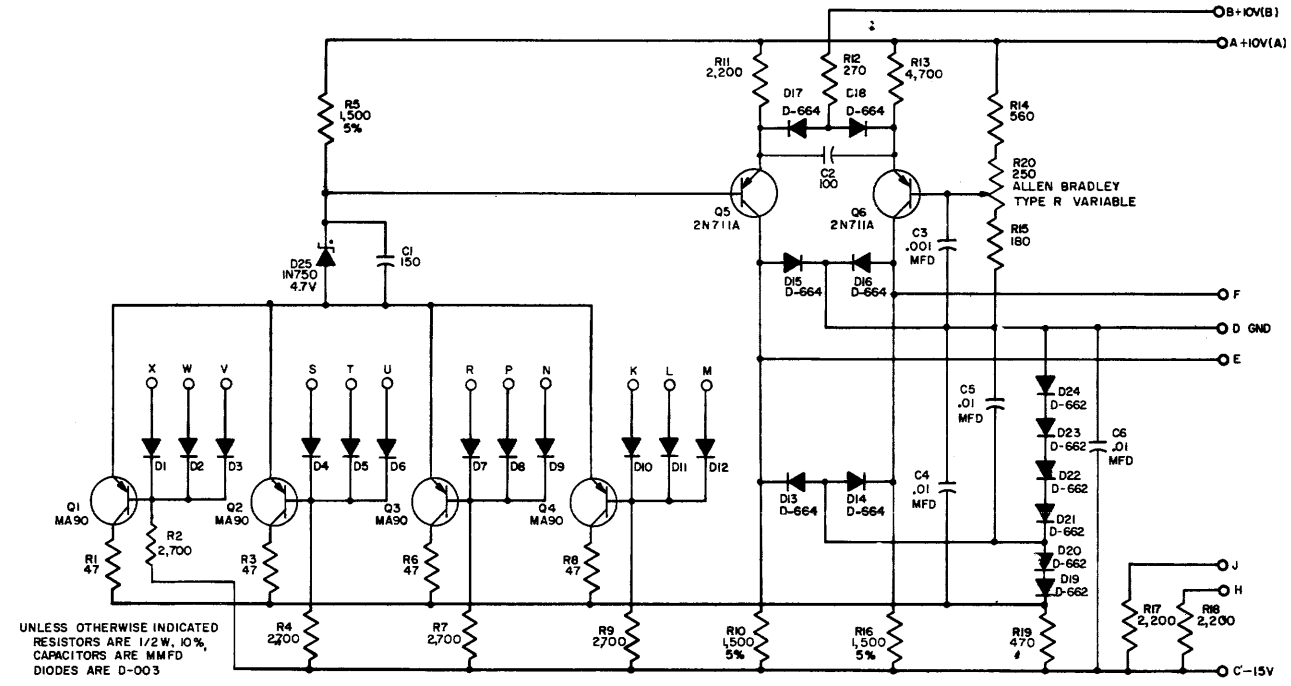

AGA RELAY DEB-11
DELAYED ON 728 -15V
1
3
M
2
4
M
20 MINUTE TIME DELAY
IN WAVE FILTER
BOTTOM VIEW OF AGASTAT RELAY



UNLESS OTHEWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MFD
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-664	IN3605		
D-662	IN645		

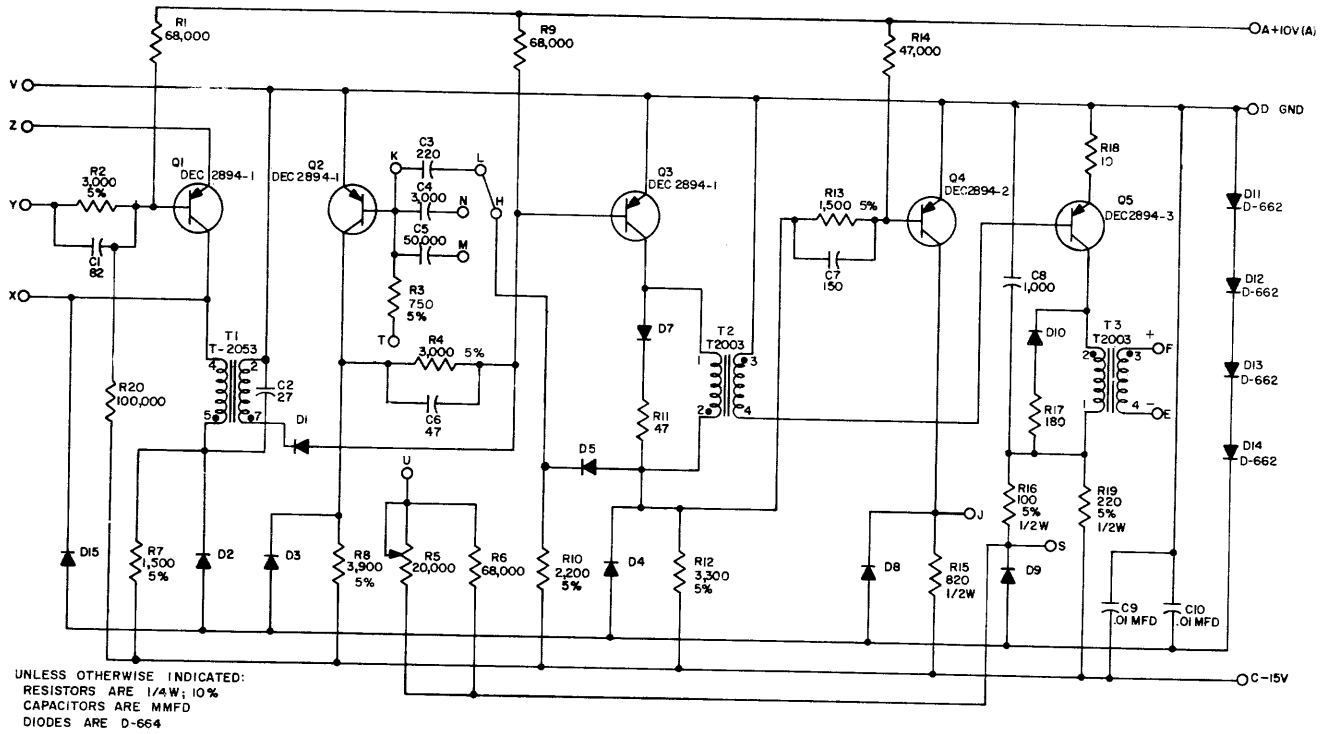
Clamped Load Resistors RS-1000



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/2W, 10%,
CAPACITORS ARE MMFD
DIODES ARE D-003

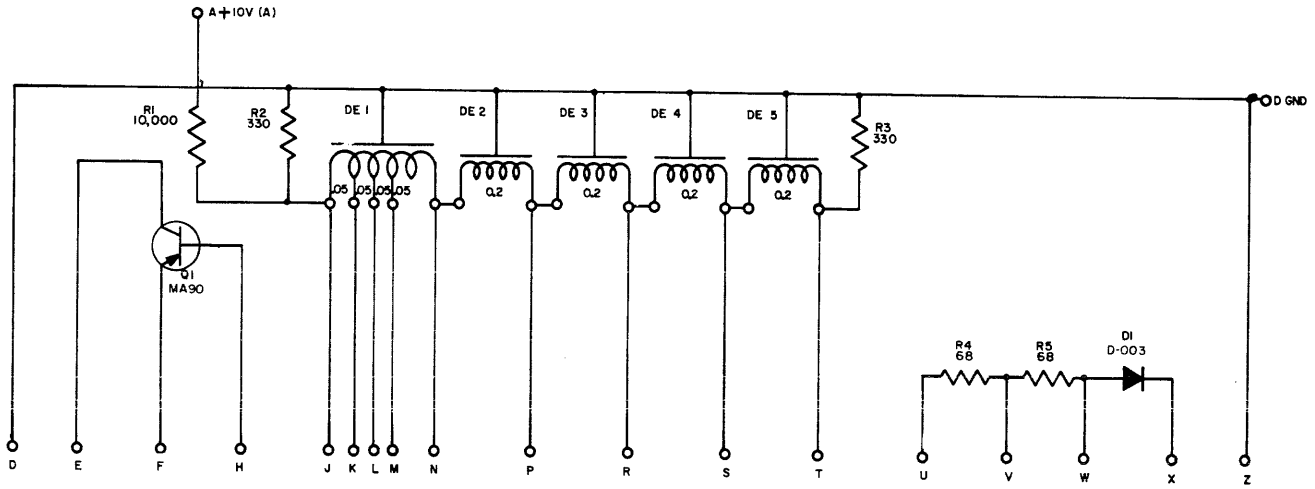
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA90	2N2451	IN750 4.7V	IN750 4.7V
2N711A	2N711A		
D-003	IN994		
D-662	IN645		
D-664	IN914		

Three-Bit Parity Circuit RS-1130



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC2894		
DEC2894-2	DEC2894		
DEC2894-3	DEC2894		
D-662	IN645		
D-664	IN3606		

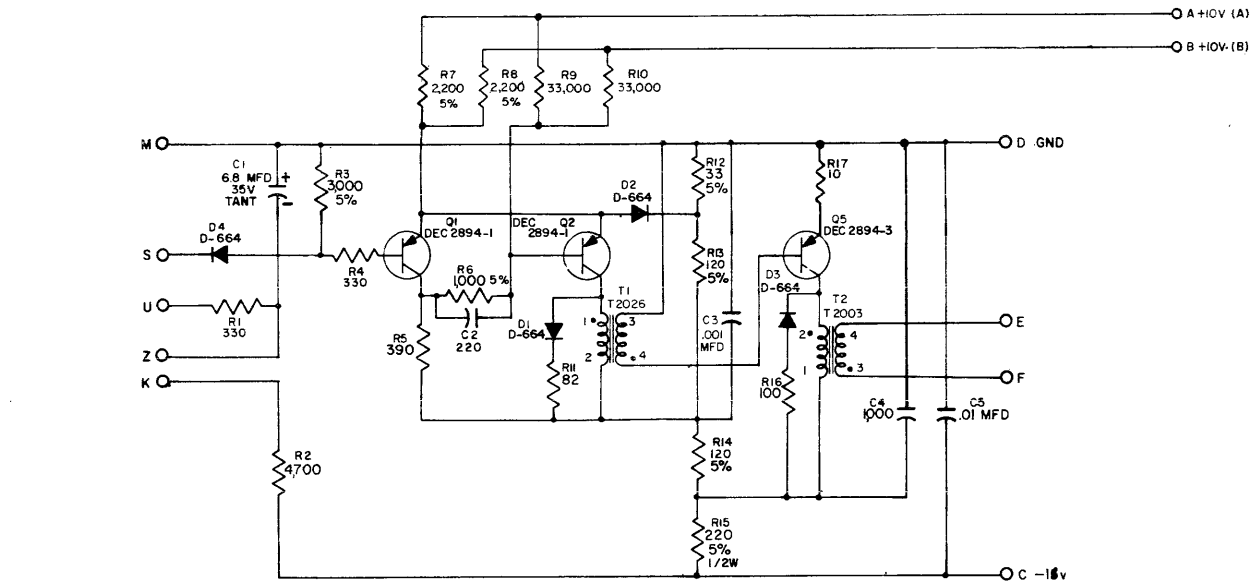
Delay RS-1304



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/2W; 10%
DE1= TECHNITROL 0.2 μ sec DELAY LINE 330 OHMS
TAPPED AT 0.05 μ sec. INTERVAL
DE2= DE5 TECHNTROL 0.2 μ sec. DELAY LINE

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA90	2N2451		
D-003	IN994		

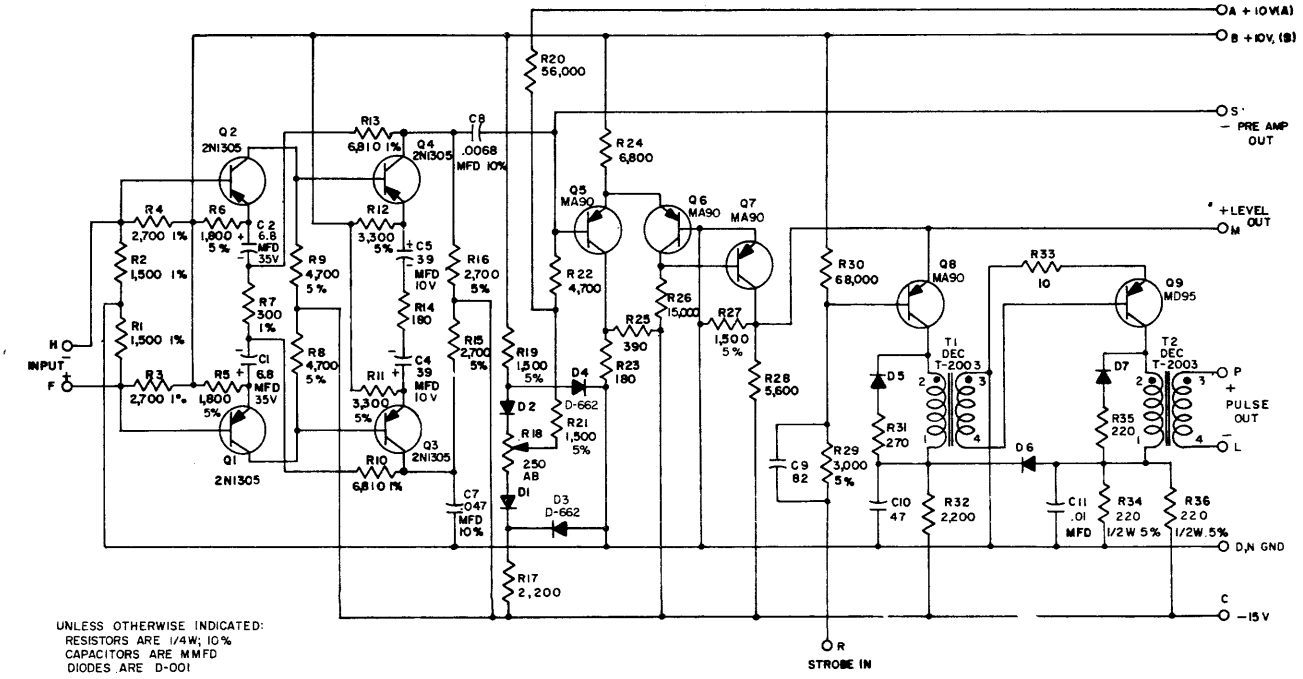
Delay Line RS-1310



UNLESS OTHEWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC 2894		
DEC 2894-3	DEC 2894		
D-664	1N914		

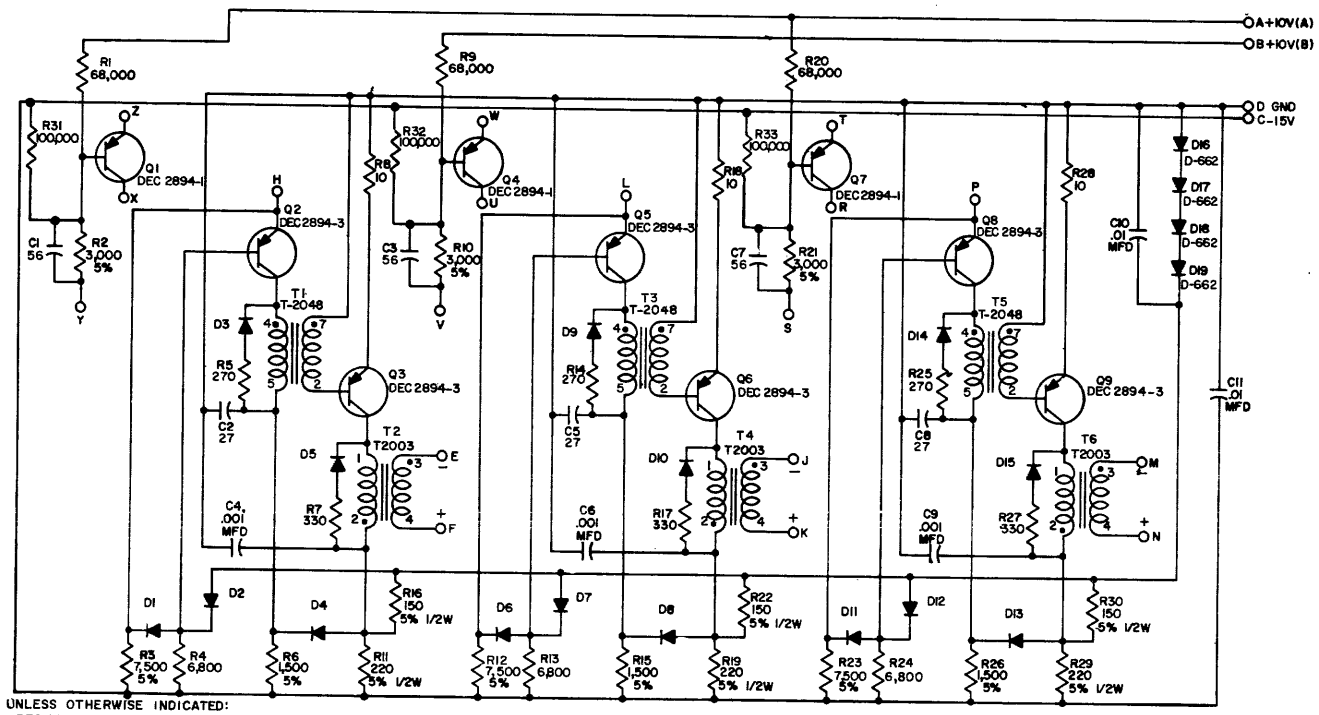
Pulse Generator RS-1410



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD
DIODES ARE D-001

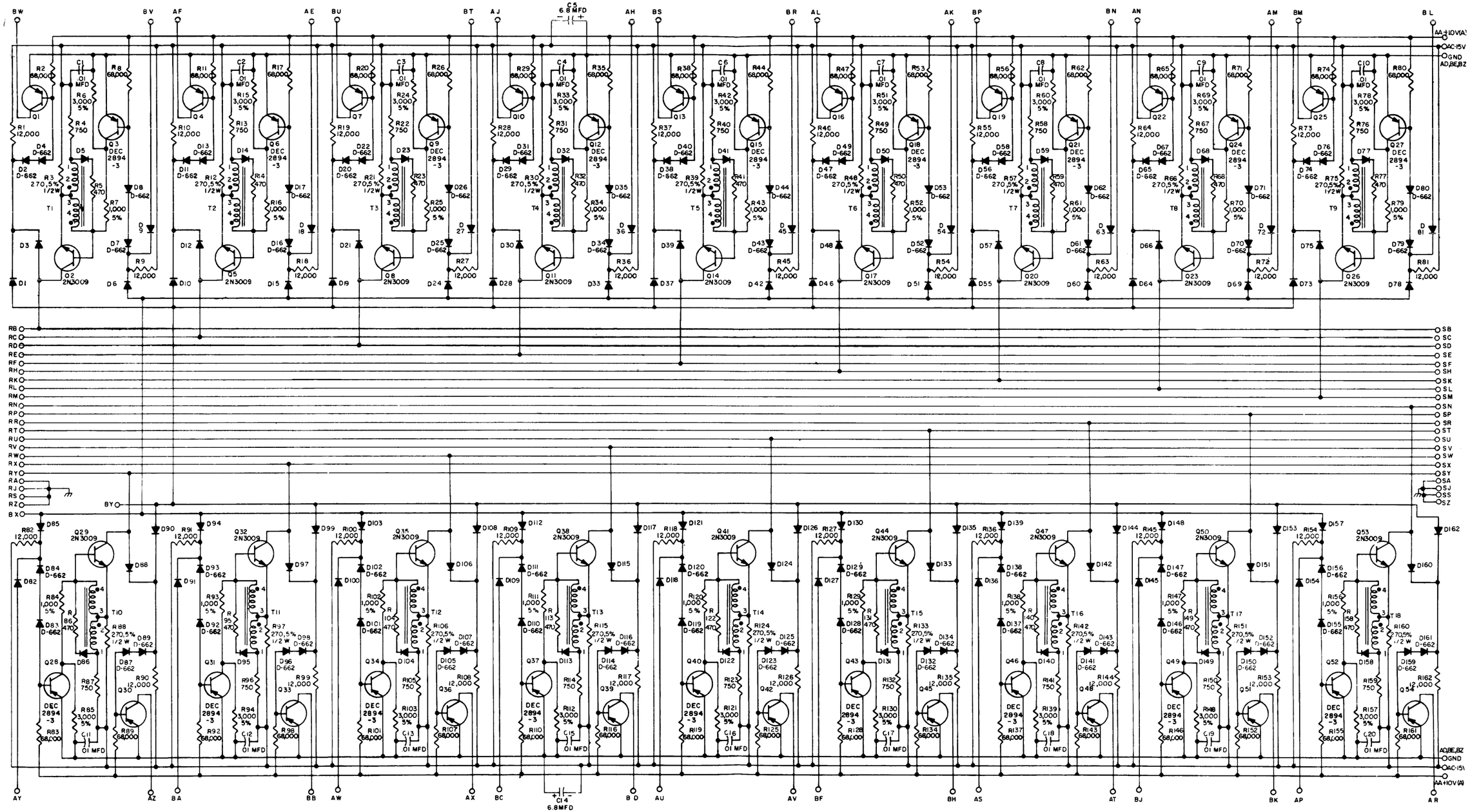
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MA90	2N2451		
MD95	2N2489		
2N1305	2N1305		
D-001	1N276		
D-662	1N645		

Drum Sense Amplifier RS-1537



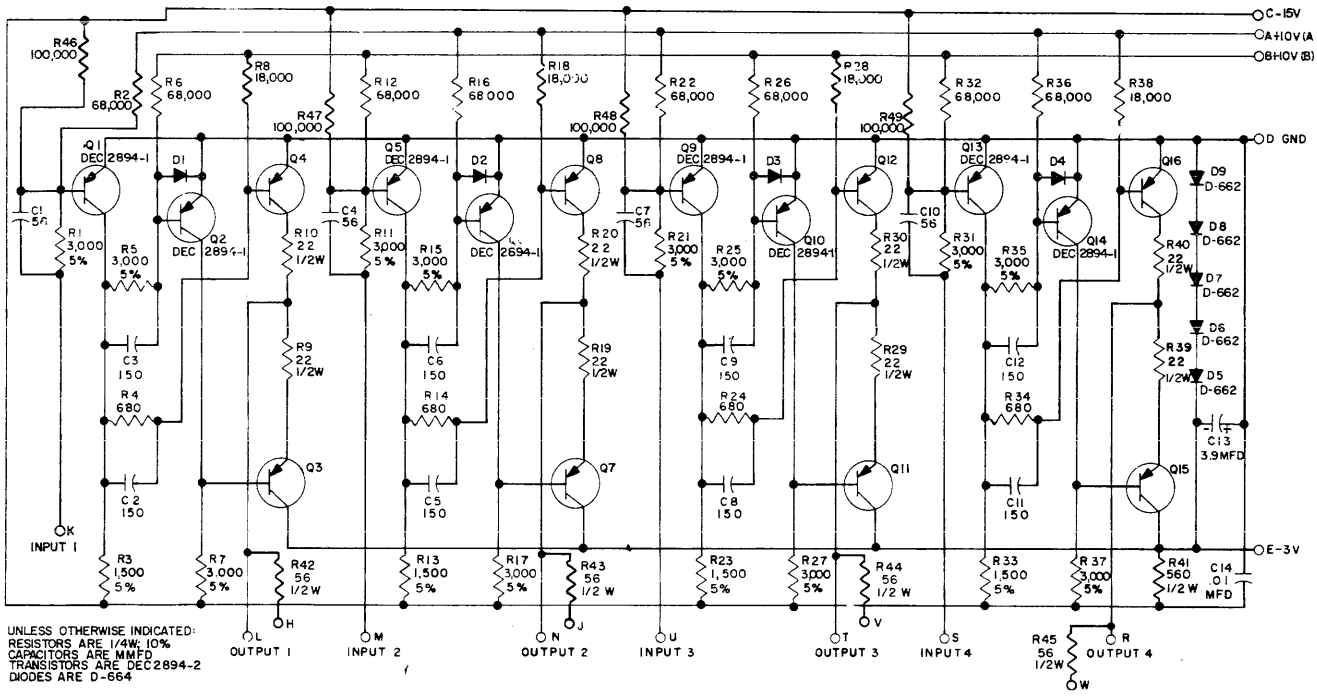
UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W, 10 %
CAPACITORS ARE MMFD
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-I	DEC2894		
DEC 2894-3	DEC 2894		
D-664	1N914		
D-662	1N645		



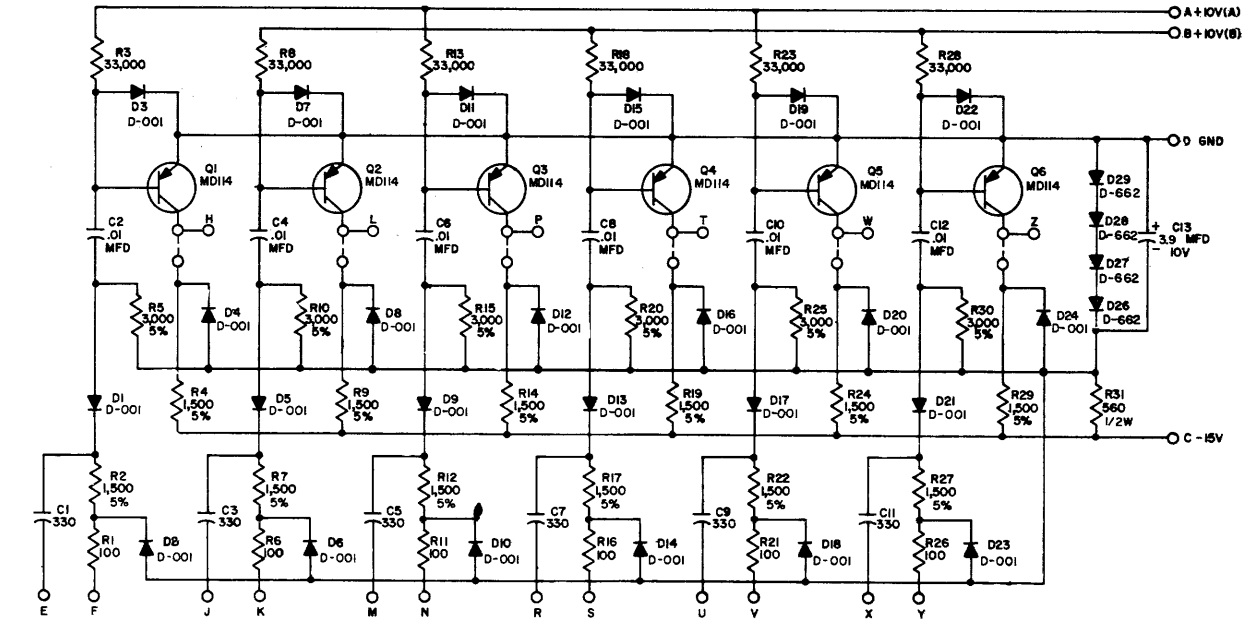
* UNLESS OTHERWISE INDICATED:
TRANSFORMERS ARE T-2044
DIODES ARE D-664
RESISTORS ARE 1/4W, 10%
TRANSISTORS ARE DEC 2894-1

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1 2N5009	DEC 2894 2N3009		
D-662	IN540 IN3606		
DEC 2894-3	DEC 2894		



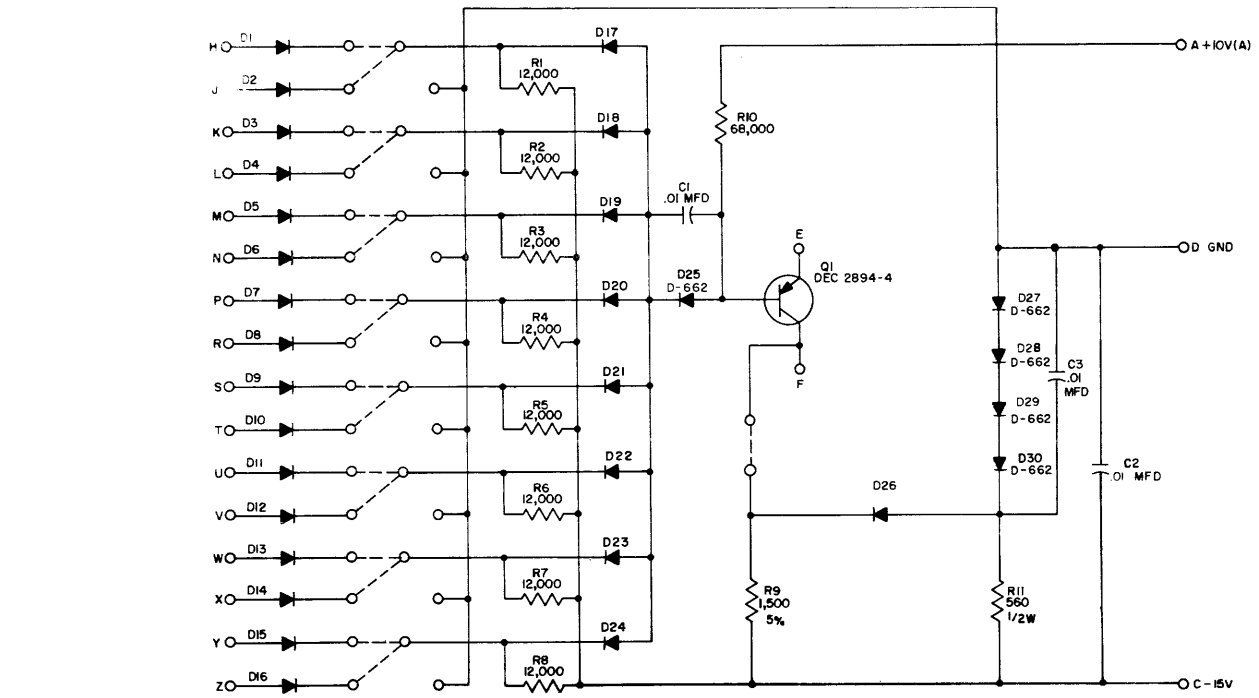
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	DEC 2894		
DEC 2894-2	DEC 2894		
D-664	IN914		
D-662	IN645		

Bus Driver RS-1684



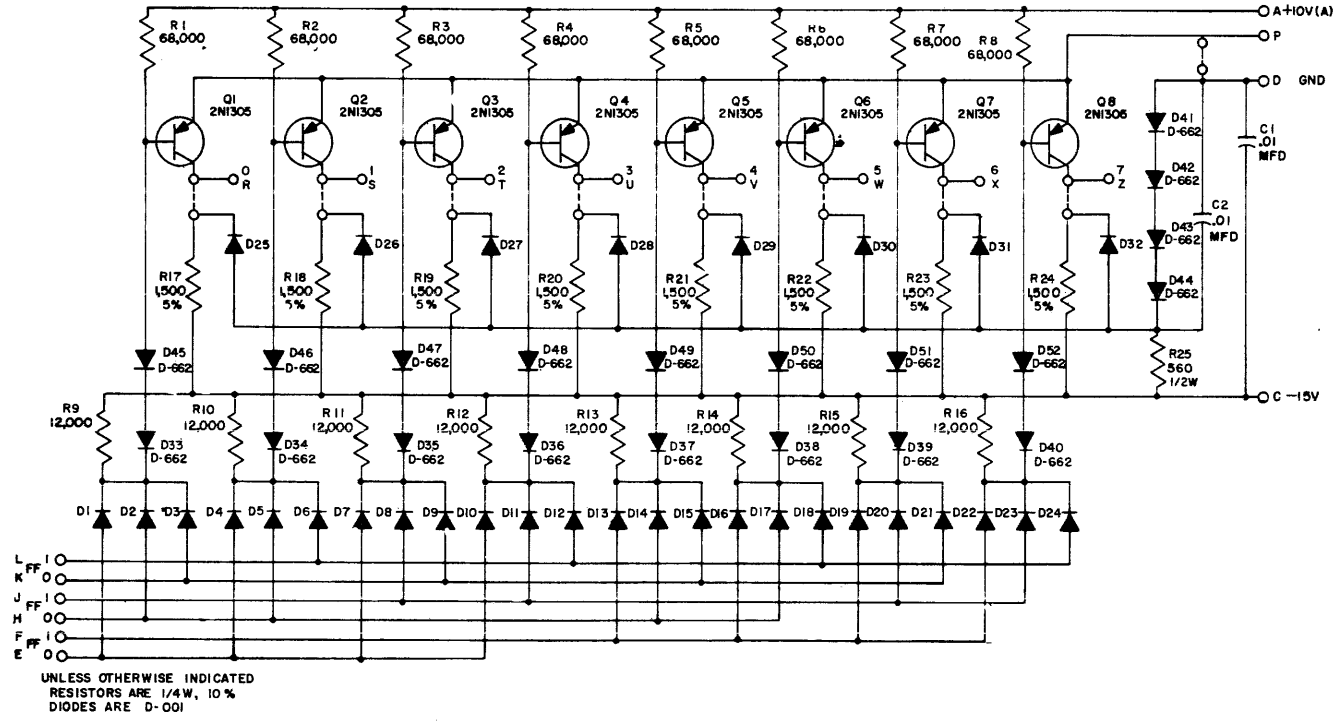
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MDI14	2N1499A		
D-001	IN276		
D-662	IN645		

Capacitor-Diode-Inverter RS-4127



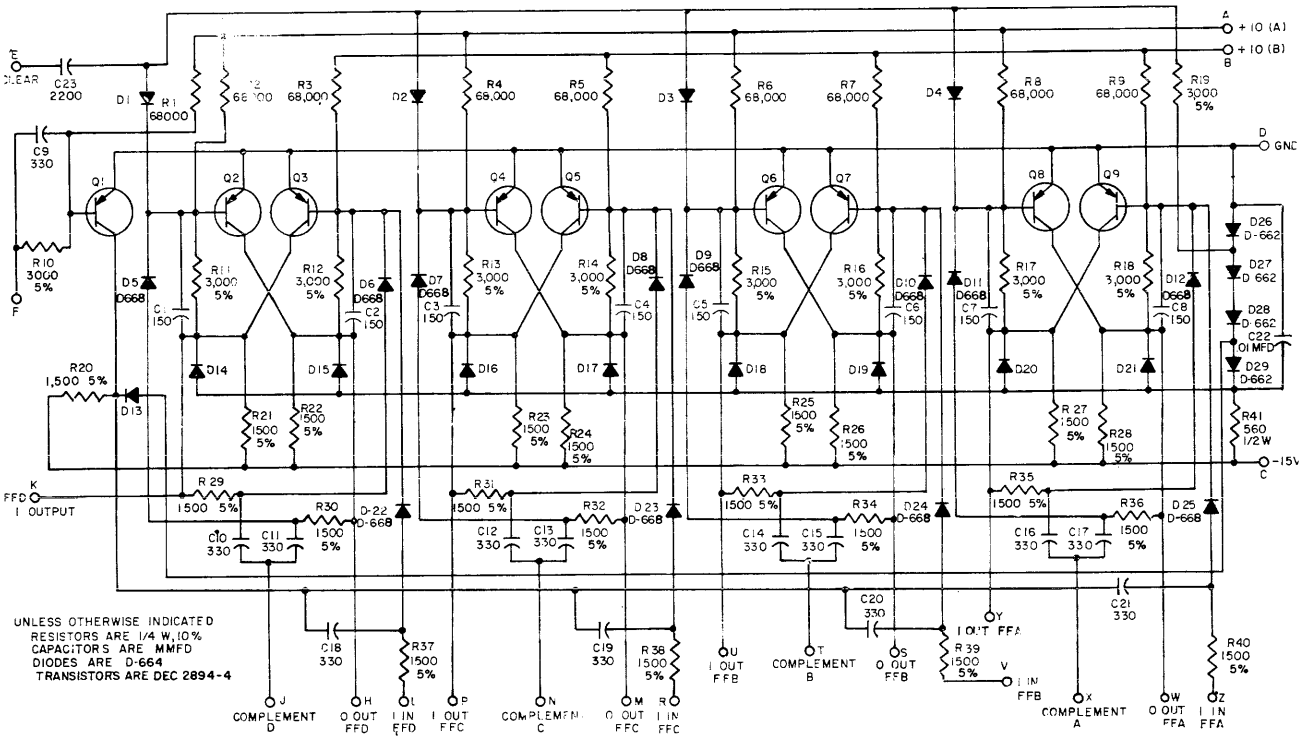
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-662	IN645		
D-664	IN3606		

Diode Unit RS-4141



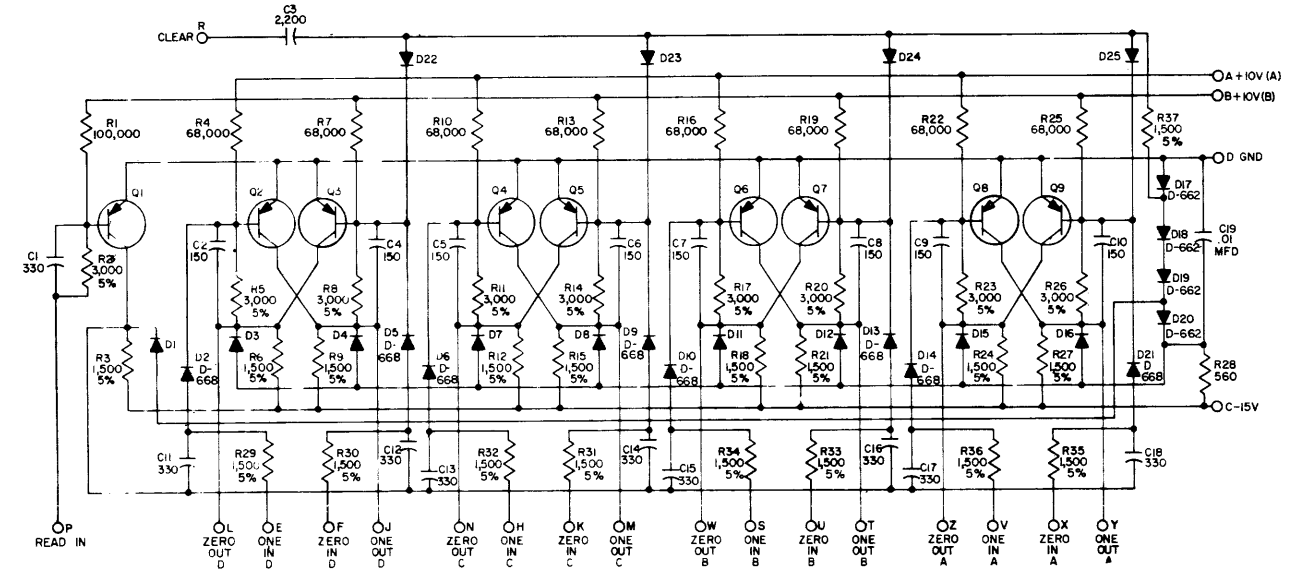
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N1305	2N1305		
D-001	IN276		
D-662	IN645		

Binary-to-Octal Decoder RS-4151



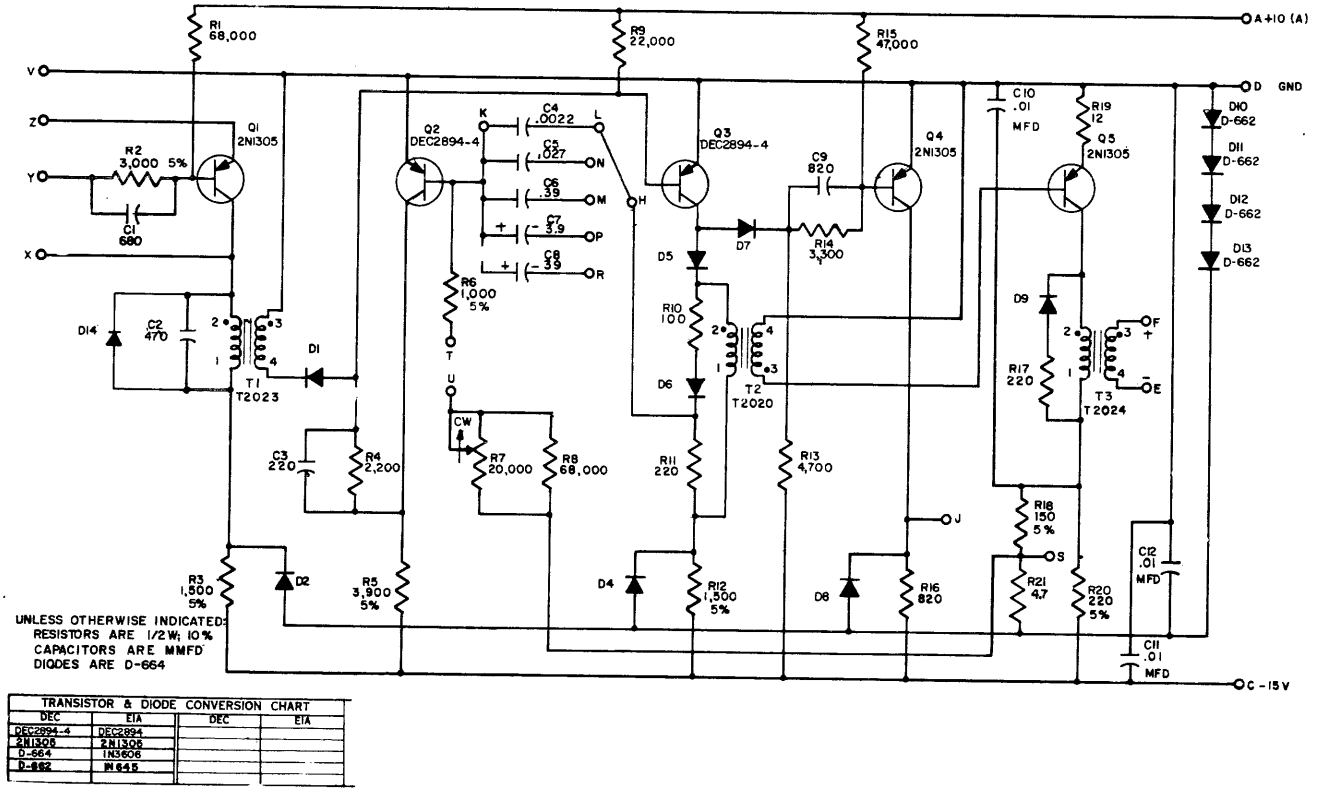
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-668	D-668*		
D-662	IN645		
D-664	IN3606		

Four-Bit Counter RS-4217



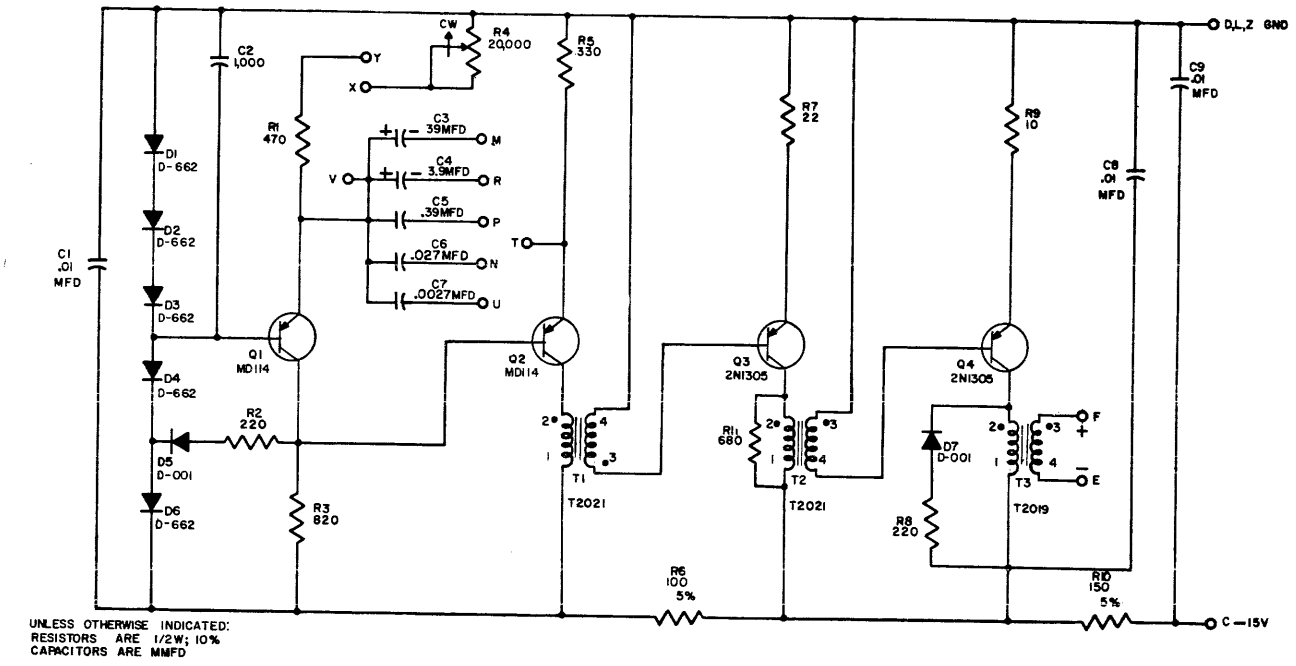
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-4	DEC 2894		
D-664	IN3606		
D-662	IN645		
D-668	D-668*		

Quadruple Flip-Flop RS-4218



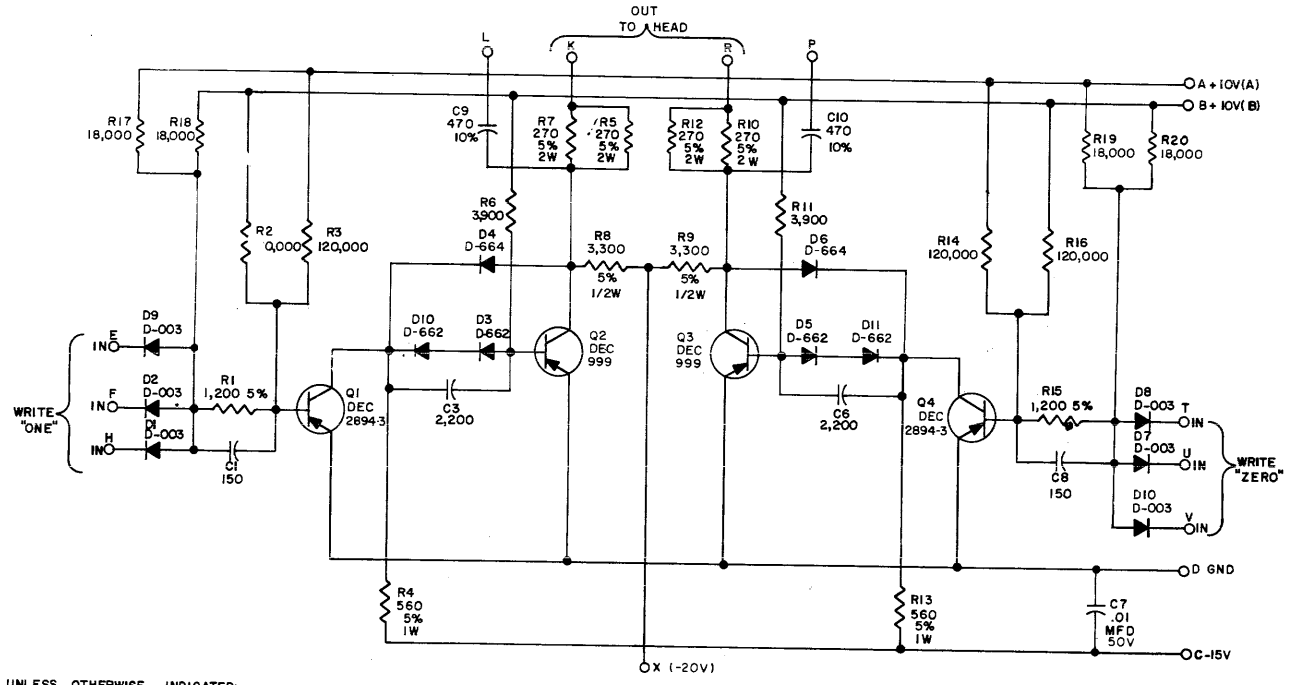
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-4	DEC2894		
2N1305	2N1305		
D-664	IN3606		
D-662	IN645		

Delay RS-4301



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
MD114	2N1499A		
2N1305	2N1305		
D-001	IN276		
D-662	IN645		

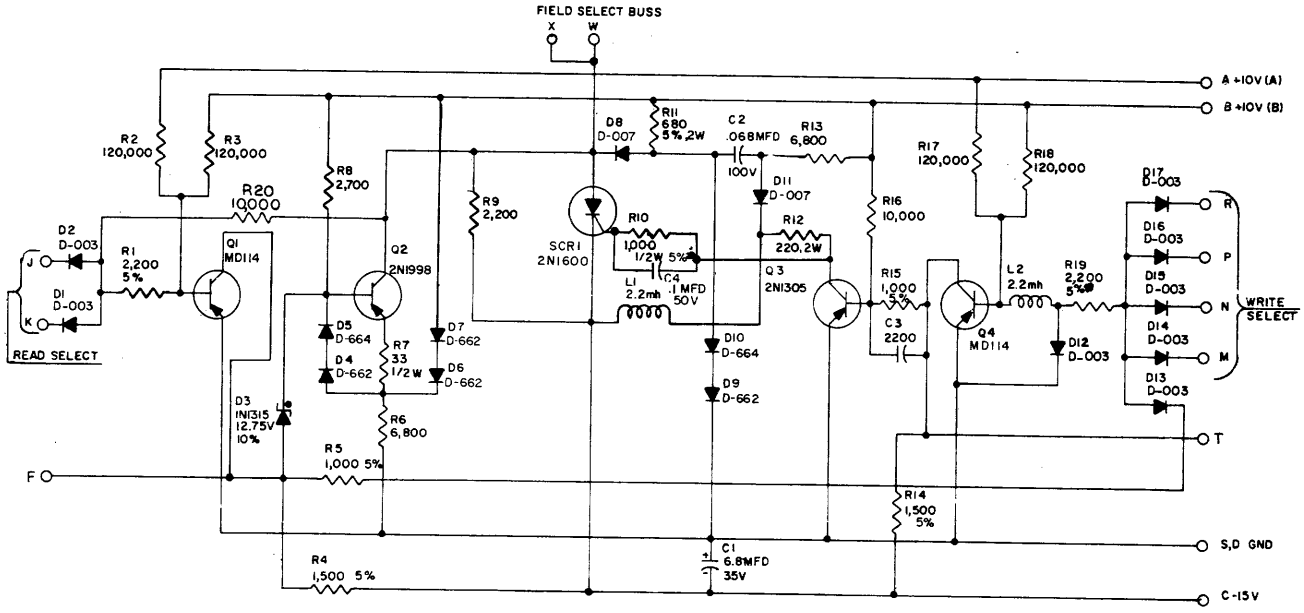
Clock RS-4401



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-003	IN994		
DEC 2894-3	DEC 2894		
D-662	IN645		
DEC999	MM999		
D-664	IN3606		

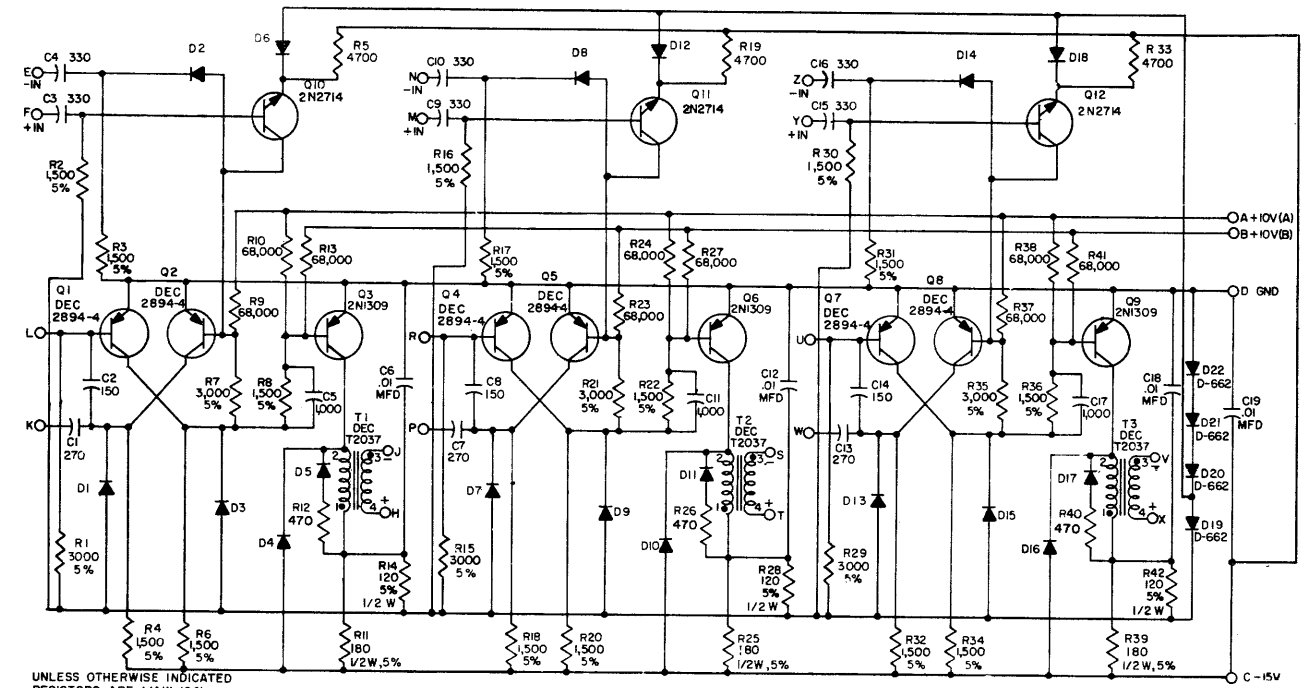
Drum NRZ Writer RS-4518



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4W; 10%
CAPACITORS ARE MMFD

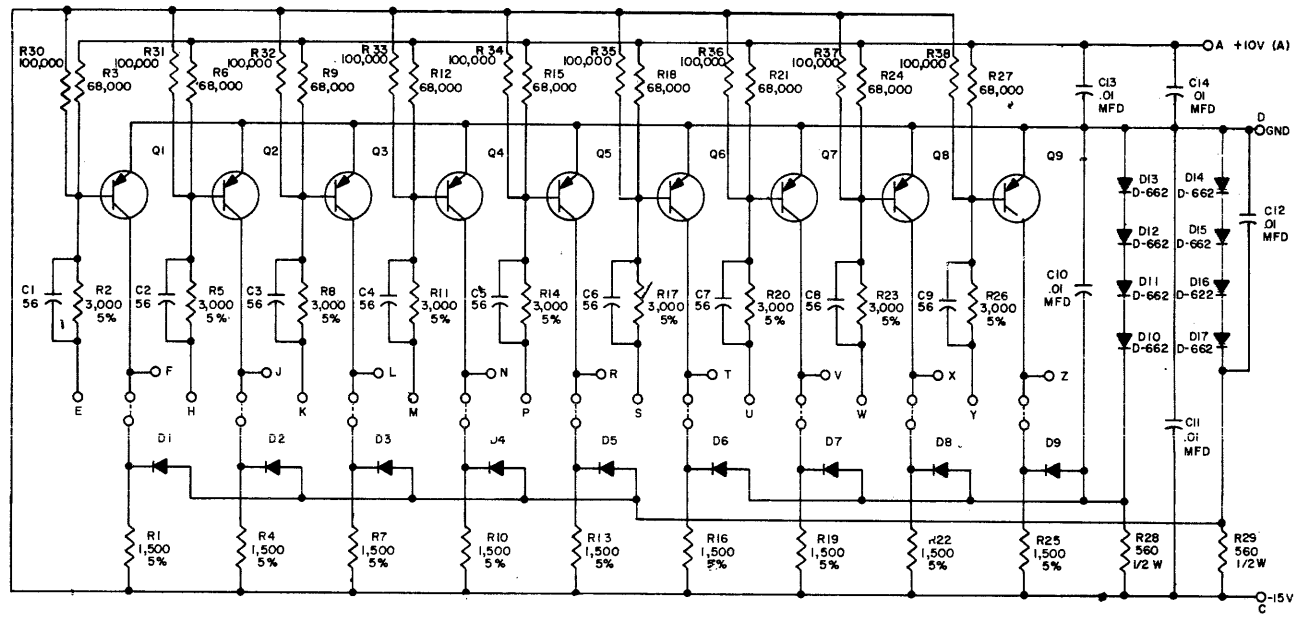
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
D-003	IN994	MD114	2N1499A
D-007	IN277	2N1305	2N1305
D-662	IN645	2N1998	2N1998
D-664	IN3605	2N1600	2N1600
IN1315	IN1315		

Drum Field Select RS-4519



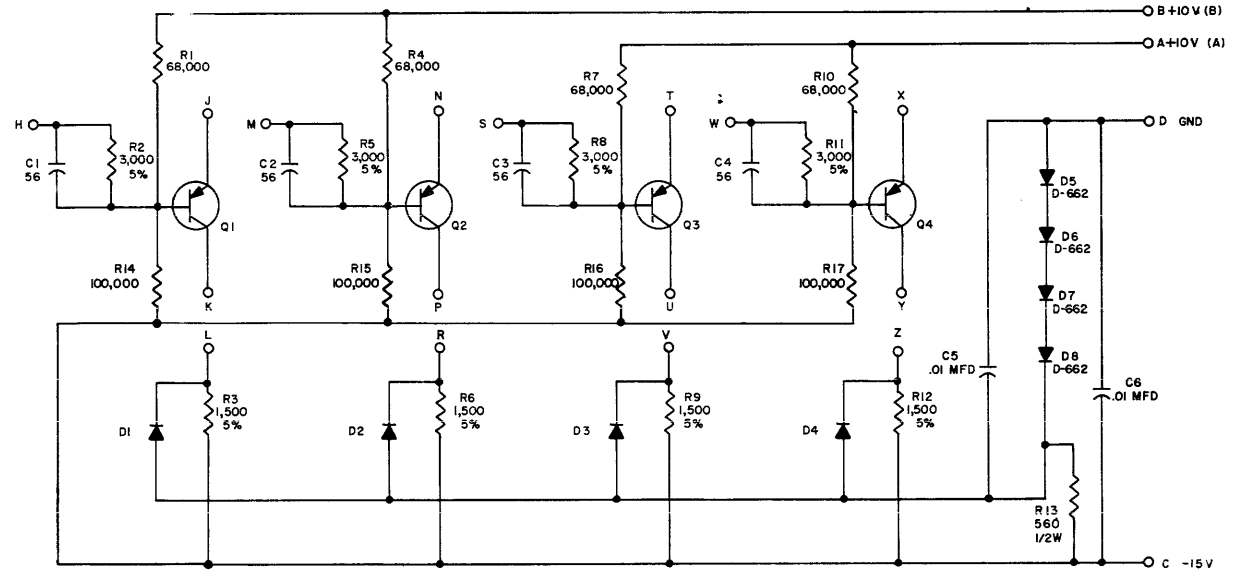
TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
2N2714	2N2714		
DEC 2894-4	DEC 2894		
2N1309	2N1309		
D-664	IN3606		
D-662	IN645		

Pulse Amplifier RS-4604



TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	2N2894		
D-664	IN914		
D-662	IN645		

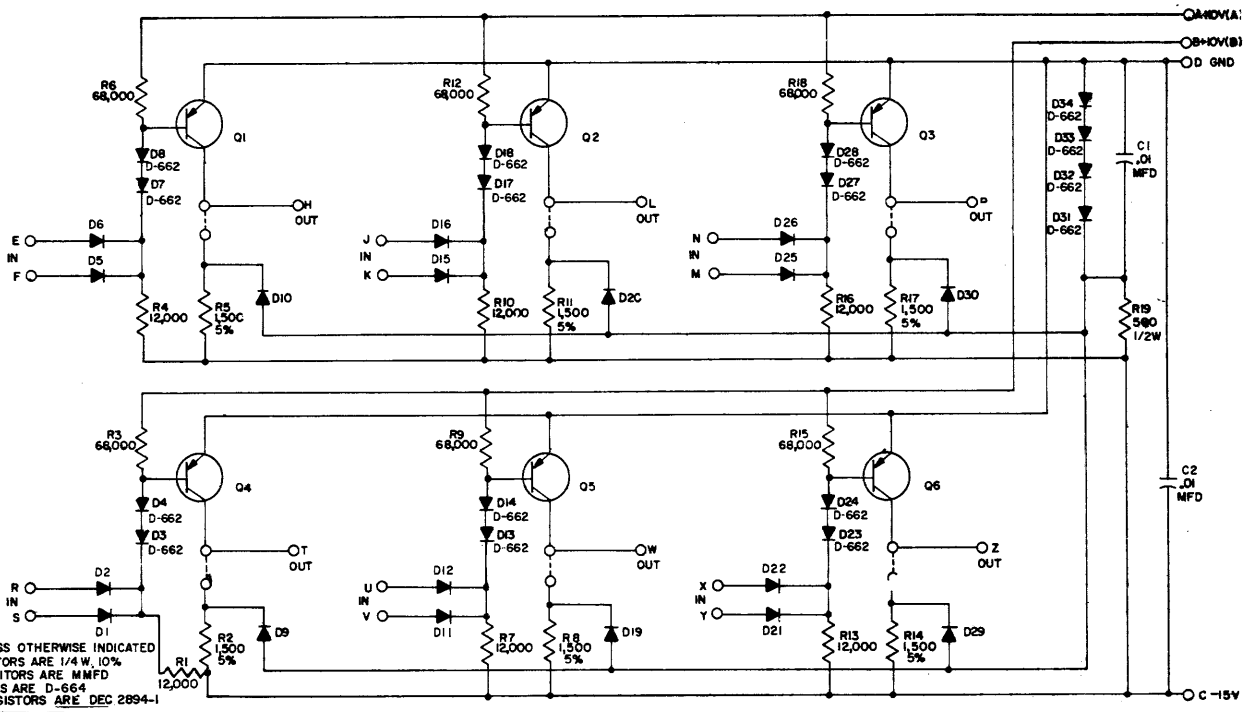
Inverter RS-6102



UNLESS OTHERWISE INDICATED:
RESISTORS ARE 1/4 W; 10%
CAPACITORS ARE MMFD
TRANSISTORS ARE DEC 2894-1
DIODES ARE D-664

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC2894-1	2N2894		
D-662	IN645		
D-664	IN914		

Inverter RS-6104



UNLESS OTHERWISE INDICATED
RESISTORS ARE 1/4 W, 10%
CAPACITORS ARE MMFD
DIODES ARE D-664
TRANSISTORS ARE DEC 2894-1

TRANSISTOR & DIODE CONVERSION CHART			
DEC	EIA	DEC	EIA
DEC 2894-1	DEC2894		
D-664	IN914		
D-662	IN645		

Diode Unit RS-6113

Utilization Module List UML-D-23-0-7

(Sheet 1)

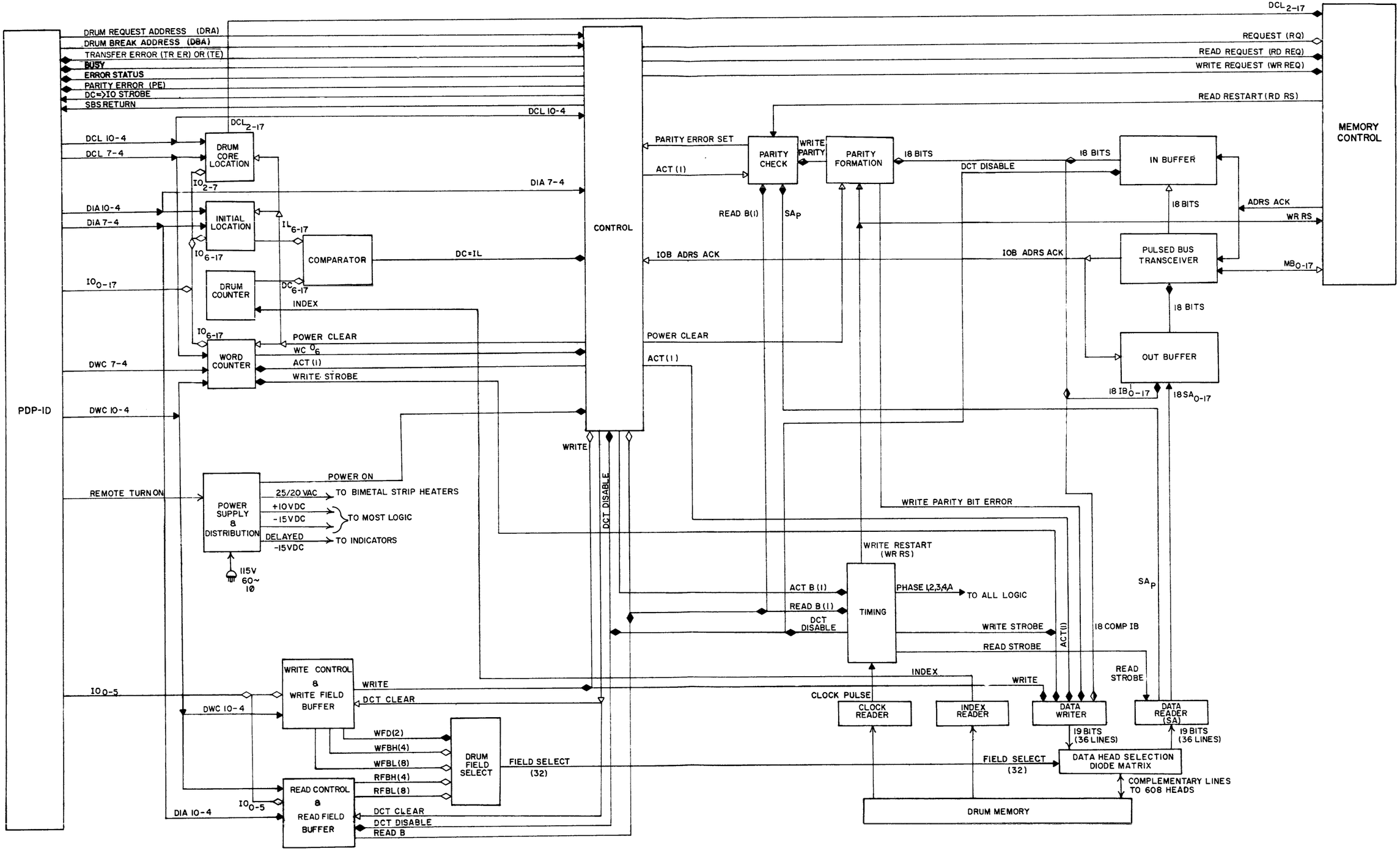
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
		4518	4518	4518	4518	4518	4518	4518	4518	4518	4518	6102R	6113R	6113R	6113R	6102R	4518	4518	4518	4518	4518	4518	4518	4518	4518
IB		WRITE PAR	WRITE 0	WRITE 1	WRITE 2	WRITE 3	WRITE 4	WRITE 5	WRITE 6	WRITE 7	WRITE 8	WRITE 0 WRITE 1 WRITE 2 WRITE 3 WRITE 4 WRITE 5 WRITE 6 WRITE 7 WRITE 8	IB0 -> WR0 IB1 -> WR1 IB2 -> WR2 IB3 -> WR3 IB4 -> WR4 IB5 -> WR5	IB6 -> WR6 IB7 -> WR7 IB8 -> WR8 IB9 -> WR9 IB10 -> WR10 IB11 -> WR11	IB12 -> WR12 IB13 -> WR13 IB14 -> WR14 IB15 -> WR15 IB16 -> WR16 IB17 -> WR17	WRITE 9 WRITE 10 WRITE 11 WRITE 12 WRITE 13 WRITE 14 WRITE 15 WRITE 16 WRITE 17	WRITE 9	WRITE 10	WRITE 11	WRITE 12	WRITE 13	WRITE 14	WRITE 15	WRITE 16	WRITE 17
		6102R	6113R	1130	1130					4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519
IC		L1-WR PAR WRITE STROBE WRITE ENABLE	PARITY DECISION WRITE STROBE WRITE ENABLE	PARITY	PARITY					FIELD SELECT 0	FIELD SELECT 1	FIELD SELECT 2	FIELD SELECT 3	FIELD SELECT 4	FIELD SELECT 5	FIELD SELECT 6	FIELD SELECT 7	FIELD SELECT 10	FIELD SELECT 11	FIELD SELECT 12	FIELD SELECT 13	FIELD SELECT 14	FIELD SELECT 15	FIELD SELECT 16	FIELD SELECT 17
		1130	1130	1130	1130	1130	1130			4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519	4519
ID		PARITY 0-2	PARITY 3-5	PARITY 6-8	PARITY 9-11	PARITY 12-14	PARITY 15-17			FIELD SELECT 20	FIELD SELECT 21	FIELD SELECT 22	FIELD SELECT 23	FIELD SELECT 24	FIELD SELECT 25	FIELD SELECT 26	FIELD SELECT 27	FIELD SELECT 30	FIELD SELECT 31	FIELD SELECT 32	FIELD SELECT 33	FIELD SELECT 34	FIELD SELECT 35	FIELD SELECT 36	FIELD SELECT 37
			1684	1684	1684	1684	1684	6113	4217	4217	4217	4217		4604	6113R	4151	4217	4217	4217	6113R	4151	4217	4217	4217	
IE	MEMORY CONTROL PLUG	MEMORY CONTROL PLUG	WFD 1 WFD 2 SEL 0 SEL 1	SEL 2 SEL 3 DCLB 4 DCLB 5	DCLB 6 DCLB 7 DCLB 8 DCLB 9	DCLB 10 DCLB 11 DCLB 12 DCLB 13	DCLB 14 DCLB 15 DCLB 16 DCLB 17	READ PARITY I ⟶ WC READ FIELD DISABLE READ FIELD DISABLE WRITE BAD PARITY I ⟶ PE	DCL 2 DCL 3 DCL 4 DCL 5	DCL 6 DCL 7 DCL 8 DCL 9	DCL 10 DCL 11 DCL 12 DCL 13	DCL 14 DCL 15 DCL 16 DCL 17		CLR FLD SEL CLR DCL DRA RESTART	WFBH0 WFBH1 WFBH2 WFBH3 RD / WR / RQ READ PARITY	WFBL 0-7	WRITE WFB 1 WFB 2 WFB 3	WFB 4 WFB 5 READ RFB 1	RFB 2 RFB 3 RFB 4 RFB 5	RFBH0 RFBH1 RFBH2 RFBH3 SPARE DRUM ERROR	RFBL 0-7	WC 6 WC 7 WC 8 WC 9	WC 10 WC 11 WC 12 WC 13	WC 14 WC 15 WC 16 WC 17	

Utilization Module List UML-D-23-0-7

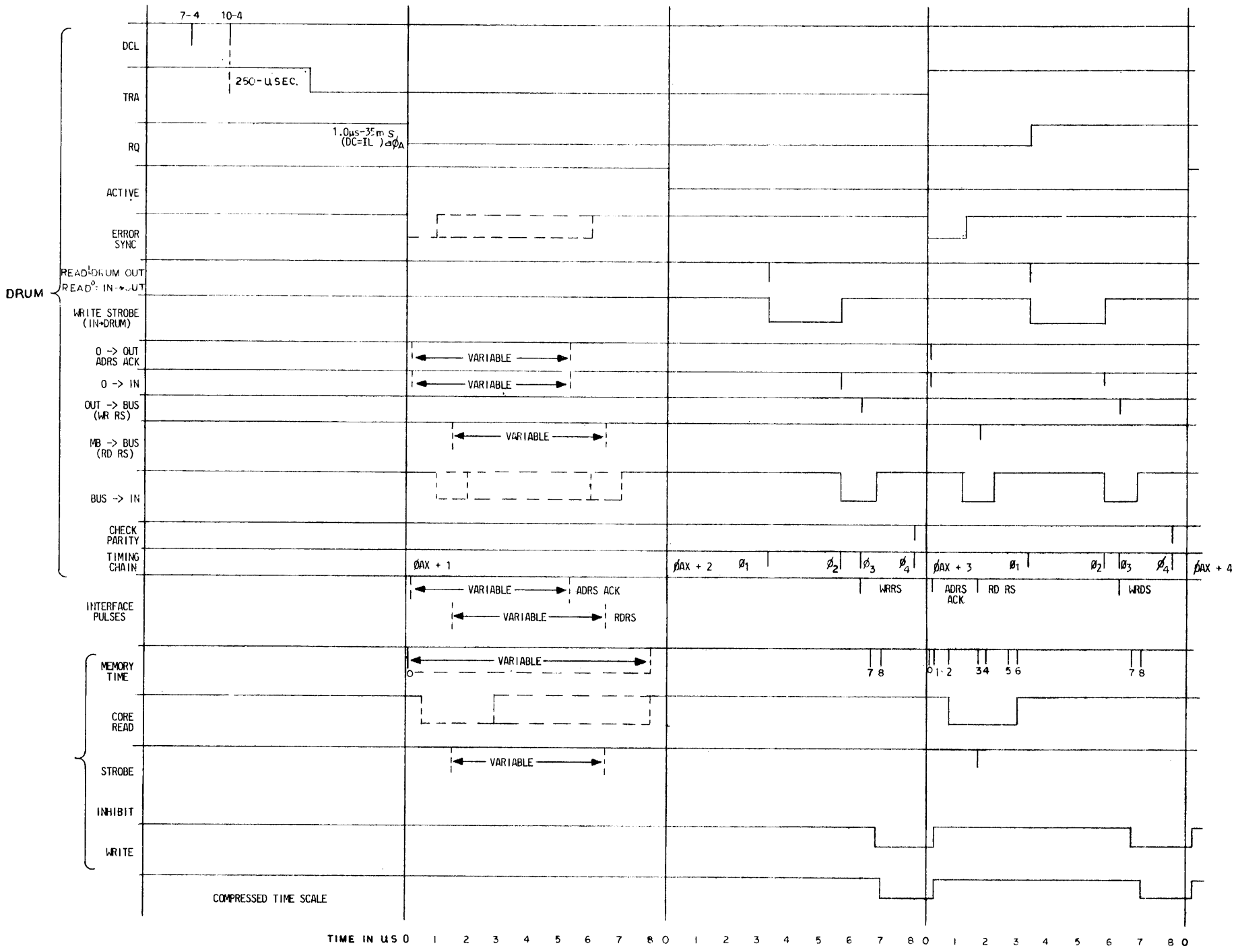
(Sheet 2)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25
		4401	1684	4604	4127	4218	6113	6102R	6102	4218	4301	4217	4141R	4217	4217	4141	4217	4217	4141	4217	4604	6102R	6102R		
1F		POWER CLEAR	RQ RD RQ SPARE WR RQ	CLEAR CONTROL SBS RETURN WR RS	READ ZERO RFB 1 WC INDEX ZERO REQ ERROR SYNC ERROR SYNC	TRA RQ ACT ER SYNC	1 → ACT WRITE PAR 1 → RQ 0 → DBA SYNC TRANS ER ER SYNC	PAR RD 1 PAR RD 0 PULL READ RQB 0 RQB 1 RD PAR 1 → RFB1 ACT RD PAR	0 PAR RD ↔ PAR RD TRA RD PAR Ø1 Ø2 Ø3 1 → DRA SYNC 1 → DBA SYNC	TRA ER PAR ER DRA SYNC DBA SYNC	TRA DELAY	DC 6 DC 7 DC 8 DC 9	COMP 6^0 COMP 6^1 COMP 7^0 COMP 7^1 COMP 8^0 COMP 8^1 COMP 9^0 COMP 9^1	IL 6 IL 7 IL 8 IL 9	DC 10 DC 11 DC 12 DC 13	COMP 10^0 COMP 10^1 COMP 11^0 COMP 11^1 COMP 12^0 COMP 12^1 COMP 13^0 COMP 13^1	IL 10 IL 11 IL 12 IL 13	DC 14 DC 15 DC 16 DC 17	COMP 14^0 COMP 14^1 COMP 15^0 COMP 15^1 COMP 16^0 COMP 16^1 COMP 17^0 COMP 17^1	IL 14 IL 15 IL 16 IL 17	CLR IL CLR WC CLR DC	COMP WC 1 READ 0 RF BB 0 RF BB 1 I → DCL INDEX DC WC 6 WC 7 WC 8	WC 9 WC 10 WC 11 WC 12 WC 13 WC 14 WC 15 WC 16 WC 17		
					1310	1304	1310	1607	6104	4604	1000	6102				4604	6102R	6102R	6102	6102R	6102R	6102		1665	
1H					TIME CHAIN	WRITE STROBE	TIME CHAIN	TIME CHAIN RD STROBE READ STROBE 0 → WRITE PE SPARE RD PAR	PHASE 1 Ø1 ENABLE PHASE 2 PHASE 3	TIME CHAIN PHASE A	BUSY 1 BUSY 0 WRITE PE 1 WRITE PE 0 WRITE PAR DISCAT D I S C A T B L E	I → BUSY BUSY 0 BUSY 1 0 → BUSY 0 → BUSY 0 → WRITE PE WRITE PE 1 WRITE PE 0 WRITE PAR				CLEAR IB IB STROBE ADR ACK	IB 0(0) IB 1(0) IB 2(0) IB 3(0) IB 4(0) IB 5(0) IB 6(0) IB 7(0) IB 8(0)	IB 0(1) IB 1(1) IB 2(1) IB 3(1) IB 4(1) IB 5(1) IB 6(1) IB 7(1) IB 8(1)	0 1 CLEAR IB 2 3 4 5 6 7 8	IB 9(0) IB 10(0) IB 11(0) IB 12(0) IB 13(0) IB 14(0) IB 15(0) IB 16(0) IB 17(0)	IB 9(1) IB 10(1) IB 11(1) IB 12(1) IB 13(1) IB 14(1) IB 15(1) IB 16(1) IB 17(1)	9 10 CLEAR IB 11 12 13 14 15 16 17		PULSED BUS	
											4604	6102	6102R	6102R	6102	4127	4127	4127	6102	6102R	6102R	6102			
1J											CLR OB IB+OB OB OUT	SA-OB 0 1 2 3 4 5 6 7 8	OB 0^0 OB 1^0 OB 2^0 OB 3^0 OB 4^0 OB 5^0 OB 6^0 OB 7^0 OB 8^0	OB 0^1 OB 1^1 OB 2^1 OB 3^1 OB 4^1 OB 5^1 OB 6^1 OB 7^1 OB 8^0	CLEAR OB OB 8^1	0 IB 1 2 3 OB 4 5	6 IB 7 8 9 OB 10 11	12 IB 13 14 15 OB 16 17	9 SA 10 11 12 13 14 OB 15 16 17	OB 9^0 OB 10^0 OB 11^0 OB 12^0 OB 13^0 OB 14^0 OB 15^0 OB 16^0 OB 17^0	OB 9^1 OB 10^1 OB 11^1 OB 12^1 OB 13^1 OB 14^1 OB 15^1 OB 16^1 OB 17^1	9 10 CLEAR OB 11 12 13 14 15 16 17		TRANSCEIVER	
		1304	1410	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537	1537
2B			INDEX DELAY	CLOCK PA	CLOCK SA	INDEX SA	SA PAR	SA 0	SA 1	SA 2	SA 3	SA 4	SA 5	SA 6	SA 7	SA 8	SA 9	SA 10	SA 11	SA 12	SA 13	SA 14	SA 15	SA 16	SA 17

Interface and Block Diagram BD-D-23-0-17


PDP-ID
DRUM REQUEST ADDRESS (DRA)
DRUM BREAK ADDRESS (DBA)
TRANSFER ERROR (TR ER) OR (TE)
BUSY
ERROR STATUS
PARITY ERROR (PE)
DC=>IO STROBE
SBS RETURN
DCL 10-4
DCL 2-17
DCL 10-4
DCL 7-4
DRUM CORE LOCATION
IO 2-7
DIA 7-4
DIA 10-4
DIA 7-4
INITIAL LOCATION
IL 6-17
IO 6-17
COMPARATOR
DC=IL
IO 0-17
DRUM COUNTER
DC 6-17
INDEX
IO 6-17
POWER CLEAR
WC 0 6
ACT (1)
WRITE STROBE
DWC 7-4
WORD COUNTER
DWC 10-4
CONTROL
WRITE
DCT DISABLE
REMOTE TURN ON
POWER SUPPLY & DISTRIBUTION
POWER ON
25/20 VAC
TO BIMETAL STRIP HEATERS
+10 VDC
-15 VDC
TO MOST LOGIC
DELAYED -15 VDC
TO INDICATORS
115V 60~ 1Ø
IO 0-5
WRITE CONTROL & WRITE FIELD BUFFER
WRITE
DCT CLEAR
DWC 10-4
WFD(2)
WFBH(4)
WFBL(8)
RFBH(4)
RFBL(8)
DRUM FIELD SELECT
FIELD SELECT (32)
IO 0-5
READ CONTROL & READ FIELD BUFFER
DIA 10-4
DCT CLEAR
DCT DISABLE
READ B
DCL 2-17
REQUEST (RQ)
READ REQUEST (RD REQ)
WRITE REQUEST (WR REQ)
READ RESTART (RD RS)
MEMORY CONTROL
PARITY ERROR SET
ACT (1)
PARITY CHECK
WRITE PARITY
PARITY FORMATION
18 BITS
DCT DISABLE
18 BITS
IN BUFFER
18 BITS
ADRS ACK
WR RS
READ B(1)
SA P
IOB ADRS ACK
IOB ADRS ACK
PULSED BUS TRANSCEIVER
MB 0-17
18 BITS
POWER CLEAR
ACT(1)
OUT BUFFER
18 IB 0-17
18 SA 0-17
WRITE PARITY BIT ERROR
WRITE RESTART (WR RS)
ACT B (1)
READ B (1)
DCT DISABLE
TIMING
PHASE 1,2,3,4A
TO ALL LOGIC
WRITE STROBE
READ STROBE
ACT(1)
18 COMP IB
SA P
INDEX
WRITE
READ STROBE
CLOCK PULSE
CLOCK READER
INDEX READER
DATA WRITER
DATA READER (SA)
19 BITS (36 LINES)
19 BITS (36 LINES)
FIELD SELECT (32)
DATA HEAD SELECTION DIODE MATRIX
COMPLEMENTARY LINES TO 608 HEADS
DRUM MEMORY

Timing and Flow Diagram TFD-D-23-0-1



		DIA, DWC, DCL (TRANSFER GROUP)	DRA (REQUEST ADDRESS)	DBA (BREAK ADDRESS)
POWER CLR (COMMON)		0 -> TRA, RQ, ACT ERROR SYNC, TRANSFER ERROR, PARITY ERROR, DRA SYNC, DBA SYNC, BUSY, WRITE, WRITE FIELD BUFFER, READ, READ FIELD BUFFER, WC, IL, DCL		
DRA	7-4		1 -> DRA SYNC	
DIA/DBA	7-4	0 -> TRA, RQ, ACT, ERROR SYNC, TRANSFER ERROR PARITY ERROR, DRA SYNC, DBA SYNC, WRITE, WRITE FIELD, READ, READ FIELD, IL, BUSY		0 -> IL; 1 -> DBA SYNC
	10-4	IO -> READ, READ FIELD, IL		IO -> IL
DWC	7-4	0 -> WC		
	10-4	IO -> WRITE, WRITE FIELD; $\overline{IO}$ -> WC		
DCL	7-4	1 -> WC; 0 -> DCL		
	10-4	IO -> DCL; 1 -> BUSY		
	+ 200μs	1 -> TRA		
ØAany		1 -> DC	1 -> DC; 0 -> DRA SYNC = DC -> IO (FINISH)	1 -> DC
ØAx		DC = IL		DC = IL
ØAx + 1		1 -> RQ, ERROR SYNC		0 -> DBA SYNC = SEQ BRK RETURN (FINISH)
ADRS ACK		RECEIVED / NOT RECEIVED		
		0 -> IN, OUT BUFFERS		
	+ 1.0μs	0 -> ERROR SYNC; 1 -> DCL		
	+ 1.4μs	MB -> IN; 0 -> READ PARITY		
Ø4		0 -> RQ		
ØAx + 2		1 -> ACT		
Ø1		READ¹ = READ STROBE -> OUT BUFFER; READ⁰ = IN -> OUT BUFFER		
	+ .1μs	WRITE¹ = BEGIN WRITE STROBE; 1 -> WC		
		WC6 = 1 / WC6 = 0		
Ø2		DRUM WRITE (FINISH) 0 -> IN BUFFER		
Ø3		OUT BUFFER -> BUS -> IN BUFFER WR RS (RESTART WRITE PORTION MEM CYCLE)		
Ø4		CHECK PARITY		
ØAx + 3		1 -> ERROR SYNC; 0 -> TRA / 0 -> TRA		
ADRS ACK		RECEIVED / NOT RECEIVED		
		0 -> IN, OUT BUFFERS	ØAx + 4 = 1 -> TRANSFER ERROR; 0 -> BUSY ØAx +5 = 0 -> ACT=SEQ BRK RETURN (TRANSFER ERROR)	
	+ 1.0μs	0 -> ERROR SYNC; 1 -> DCL		
	+ 1.4μs	MB -> IN; 0 -> READ PARITY		
Ø1		READ¹ = READ STROBE -> OUT BUFFER; READ⁰ = IN -> OUT BUFFER		
	+ .1μs	WRITE¹ = BEGIN WRITE STROBE; 1 -> WC		
		WC6 = 1 / WC6 = 0	0 -> RQ	
Ø2		DRUM WRITE (FINISH) 0 -> IN BUFFER	DRUM WRITE (FINISH) 0 -> IN BUFFER	
Ø3		OUT BUFFER -> BUS -> IN BUFFER WR RS (RESTART WRITE PORTION MEM CYCLE)	OUT BUF -> BUS -> IN BUFFER, WR RS	
Ø4		CHECK PARITY	CHECK PARITY	
ØAx + 4		1 -> ERROR SYNC	SEQ BRK RETURN (TRANSFER COMPLETE) 0 -> ACT 0 -> BUSY	

PDP-1 TIMING

DRUM AND MEMORY TIMING

35ms

TRA¹, ERROR SYNC¹

NOTE

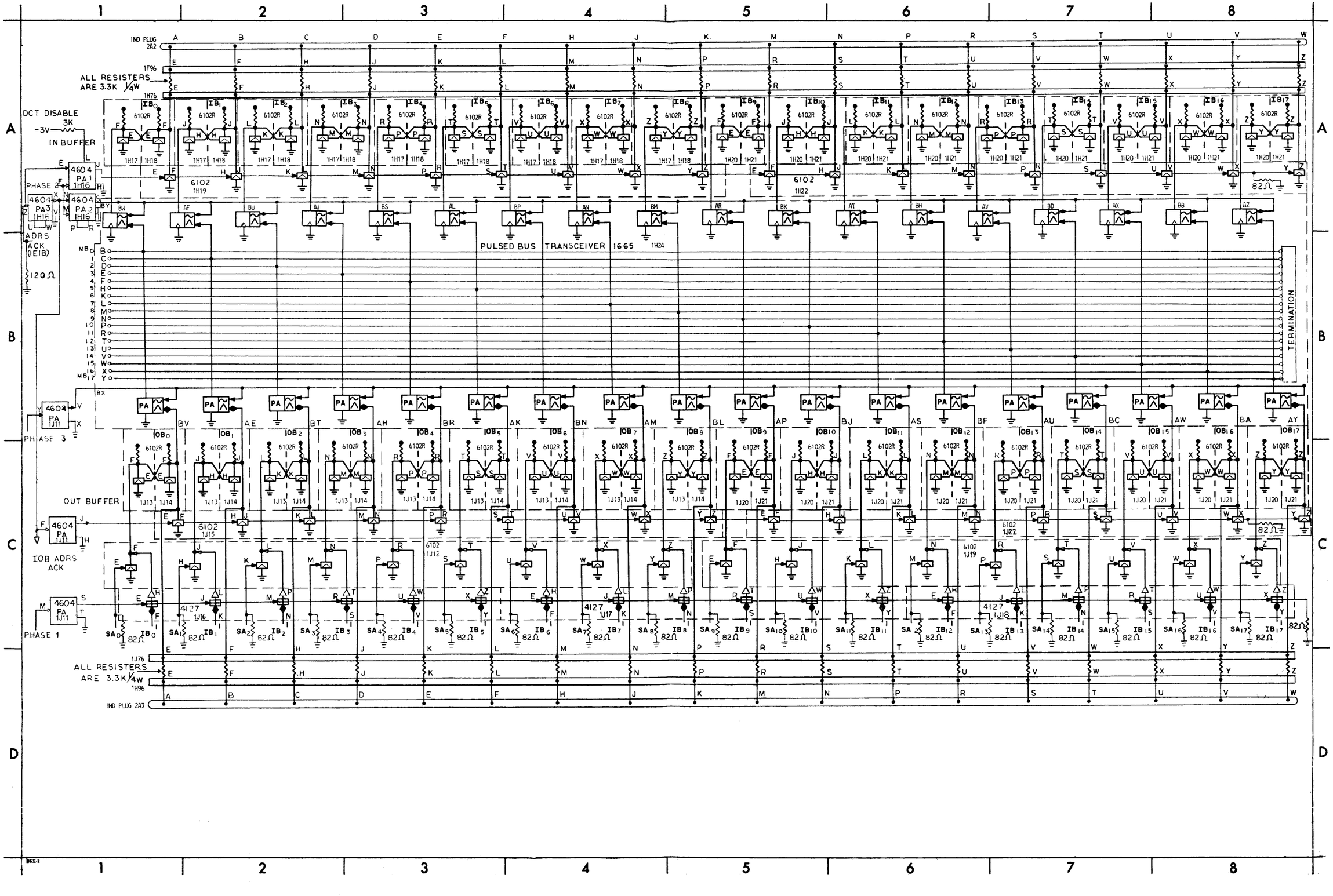
PRESSING THE WRITE BAD PARITY BUTTON (LOCATED ON FIELD LOCKOUT PANEL), WILL RESULT IN THE FIRST WORD BEING WRITTEN WITH A BAD PARITY BIT.

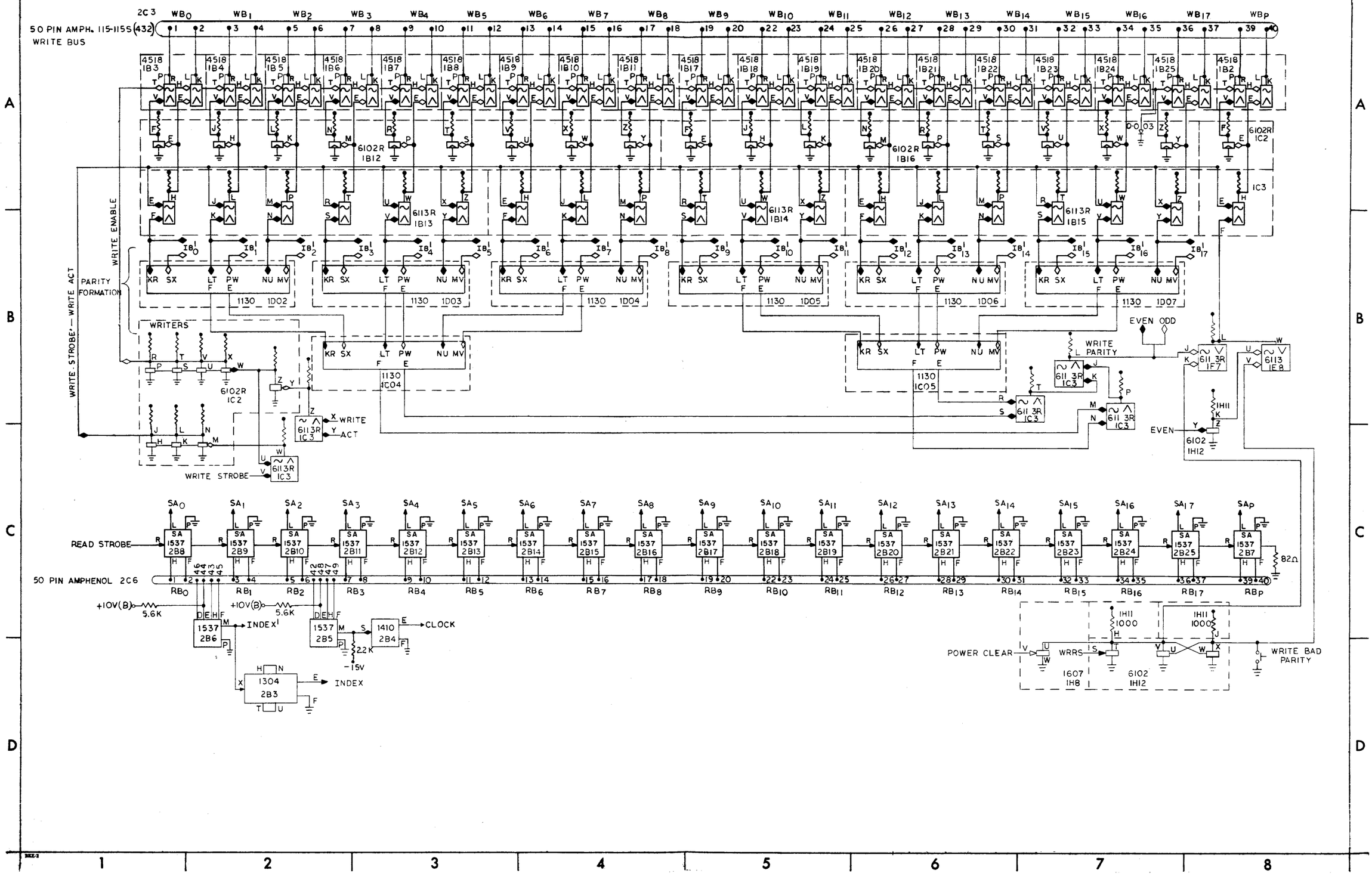
Control, Error Detection, Time Chain BS-D-23-0-2

ALL RESISTORS 3.3K UNLESS OTHERWISE INDICATED

BKE 2

In Out Buffers and Pulsed Bus Transceiver BS-D-23-0-3


IND PLUG 2A2
1F96
ALL RESISTERS ARE 3.3K 1/4W
1H76
DCT DISABLE
3K
-3V
IN BUFFER
PHASE 2
PHASE 3
PHASE 1
ADRS ACK (1E1B)
120Ω
OUT BUFFER
IOB ADRS ACK
6102R
6102
4604 PA
4127
82Ω
PULSED BUS TRANSCEIVER 1665 1H24
TERMINATION
IND PLUG 2A3


2C3
50 PIN AMPH. 115-1155 (432)
WRITE BUS
WB0 WB1 WB2 WB3 WB4 WB5 WB6 WB7 WB8 WB9 WB10 WB11 WB12 WB13 WB14 WB15 WB16 WB17 WBP
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 39 40
4518 1B3
4518 1B4
4518 1B5
4518 1B6
4518 1B7
4518 1B8
4518 1B9
4518 1B10
4518 1B11
4518 1B17
4518 1B18
4518 1B19
4518 1B20
4518 1B21
4518 1B22
4518 1B23
4518 1B24
4518 1B25
4518 1B2
6102R 1B12
6102R 1B16
6102R IC2
6113R 1B13
6113R 1B14
6113R 1B15
IC3
WRITE ENABLE
WRITE . STROBE - WRITE ACT
PARITY FORMATION
IB0 IB1 IB2 IB3 IB4 IB5 IB6 IB7 IB8 IB9 IB10 IB11 IB12 IB13 IB14 IB15 IB16 IB17
KR SX LT PW NU MV
1130 1D02
1130 1D03
1130 1D04
1130 1D05
1130 1D06
1130 1D07
WRITERS
6102R IC2
6113R IC3
WRITE
ACT
WRITE STROBE
1130 1C04
1130 1C05
EVEN ODD
WRITE L PARITY
611 3R IC3
611 3R 1F7
6113 1E8
1H11
EVEN
6102 1H12
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7 SA8 SA9 SA10 SA11 SA12 SA13 SA14 SA15 SA16 SA17 SAP
SA 1537 2B8
SA 1537 2B9
SA 1537 2B10
SA 1537 2B11
SA 1537 2B12
SA 1537 2B13
SA 1537 2B14
SA 1537 2B15
SA 1537 2B16
SA 1537 2B17
SA 1537 2B18
SA 1537 2B19
SA 1537 2B20
SA 1537 2B21
SA 1537 2B22
SA 1537 2B23
SA 1537 2B24
SA 1537 2B25
SA 1537 2B7
82Ω
READ STROBE
50 PIN AMPHENOL 2C6
RB0 RB1 RB2 RB3 RB4 RB5 RB6 RB7 RB8 RB9 RB10 RB11 RB12 RB13 RB14 RB15 RB16 RB17 RBP
+10V(B)
5.6K
1537 2B6
1537 2B5
1410 2B4
INDEX
CLOCK
2.2K
-15V
1304 2B3
INDEX
POWER CLEAR
WRRS
1607 1H8
1H11 1000
6102 1H12
WRITE BAD PARITY

Read/Write Field Buffers and Field Select BS-D-23-0-5

50 PIN AMPH 2C4

RFBH 0
WFBH 0
WFD 1

4519 1C10 FS0 · 4519 1C11 FS1 · 4519 1C12 FS2 · 4519 1C13 FS3 · 4519 1C14 FS4 · 4519 1C15 FS5 · 4519 1C16 FS6 · 4519 1C17 FS7 · 4519 1C18 FS10 · 4519 1C19 FS11 · 4519 1C20 FS12 · 4519 1C21 FS13 · 4519 1C22 FS14 · 4519 1C23 FS15 · 4519 1C24 FS16 · 4519 1C25 FS17

RFBL 0 WFBL 0 · RFBL 1 WFBL 1 · RFBL 2 WFBL 2 · RFBL 3 WFBL 3 · RFBL 4 WFBL 4 · RFBL 5 WFBL 5 · RFBL 6 WFBL 6 · RFBL 7 WFBL 7 · RFBH1 WFBH1 WFBL 0 0 · RFBL 1 WFBL · RFBL 2 WFBL · RFBL 3 WFBL · RFBL 4 WFBL · RFBL 5 WFBL · RFBL 6 WFBL · RFBL 7 WFBL

WFLO 0 SW · WFLO 1 SW · WFLO 2 SW · WFLO 3 SW · WFLO 4 SW · WFLO 5 SW · WFLO 6 SW · WFLO 7 SW · WFLO 10 SW · WFLO 11 SW · WFLO 12 SW · WFLO 13 SW · WFLO 14 SW · WFLO 15 SW · WFLO 16 SW · WFLO 17 SW ◆DCT DISABLE

50 PIN AMPH. 2C4

RFBH 2
WFBH 2
WFD 2

4519 1D10 FS20 · 4519 1D11 FS21 · 4519 1D12 FS22 · 4519 1D13 FS23 · 4519 1D14 FS24 · 4519 1D15 FS25 · 4519 1D16 FS26 · 4519 1D17 FS27 · 4519 1D18 FS30 · 4519 1D19 FS31 · 4519 1D20 FS32 · 4519 1D21 FS33 · 4519 1D22 FS34 · 4519 1D23 FS35 · 4519 1D24 FS36 · 4519 1D25 FS37

RFBL 0 WFBL 0 · RFBL 1 WFBL 1 · RFBL 2 WFBL 2 · RFBL 3 WFBL 3 · RFBL 4 WFBL 4 · RFBL 5 WFBL 5 · RFBL 6 WFBL 6 · RFBL 7 WFBL 7 · RFBL 3 3 WFBL 0 0 · RFBL 1 WFBL 1 · RFBL 2 WFBL 2 · RFBL 3 WFBL 3 · RFBL 4 WFBL 4 · RFBL 5 WFBL 5 · RFBL 6 WFBL 6 · RFBL 7 WFBL 7

WFLO 20 SW · WFLO 21 SW · WFLO 22 SW · WFLO 23 SW · WFLO 24 SW · WFLO 25 SW · WFLO 26 SW · WFLO 27 SW · WFLO 30 SW · WFLO 31 SW · WFLO 32 SW · WFLO 33 SW · WFLO 34 SW · WFLO 35 SW · WFLO 36 SW · WFLO 37 SW

IA1
22 PIN AMPH. IND PLUG

ID90
ALL RESISTORS 3.3K
¼W 10% 1E70

WFBH · WFBL

WFD 1 · WFD 2

1684 1E3 · 1684 1E3

6113R 1E15 · 6113R 1E15 · 6113R 1E15 · 6113R 1E15

4151 1E16

READ (0) B (1)

6113 1E8 · 6113 1E8

6102R 1F22

6102R 1F22

IA2

ID98

1E78

RFBH · RFBL

6113R 1E20 · 6113R 1E20 · 6113R 1E20 · 6113R 1E20

4151 1E21

DCT CLEAR

4604 1E14

DWC IO-4

82Ω

WRITE · WFB 1 · WFB 2 · WFB 3 · WFB 4 · WFB 5

IO_0 IO_1 IO_2 IO_3 IO_4 IO_5

4217R 1E17

4217 1E18

READ · RFB 1 · RFB 2 · RFB 3 · RFB 4 · RFB 5

DCT DISABLE

6102R 1F8

DIA/DBA IO-4

82Ω

4127 1F5

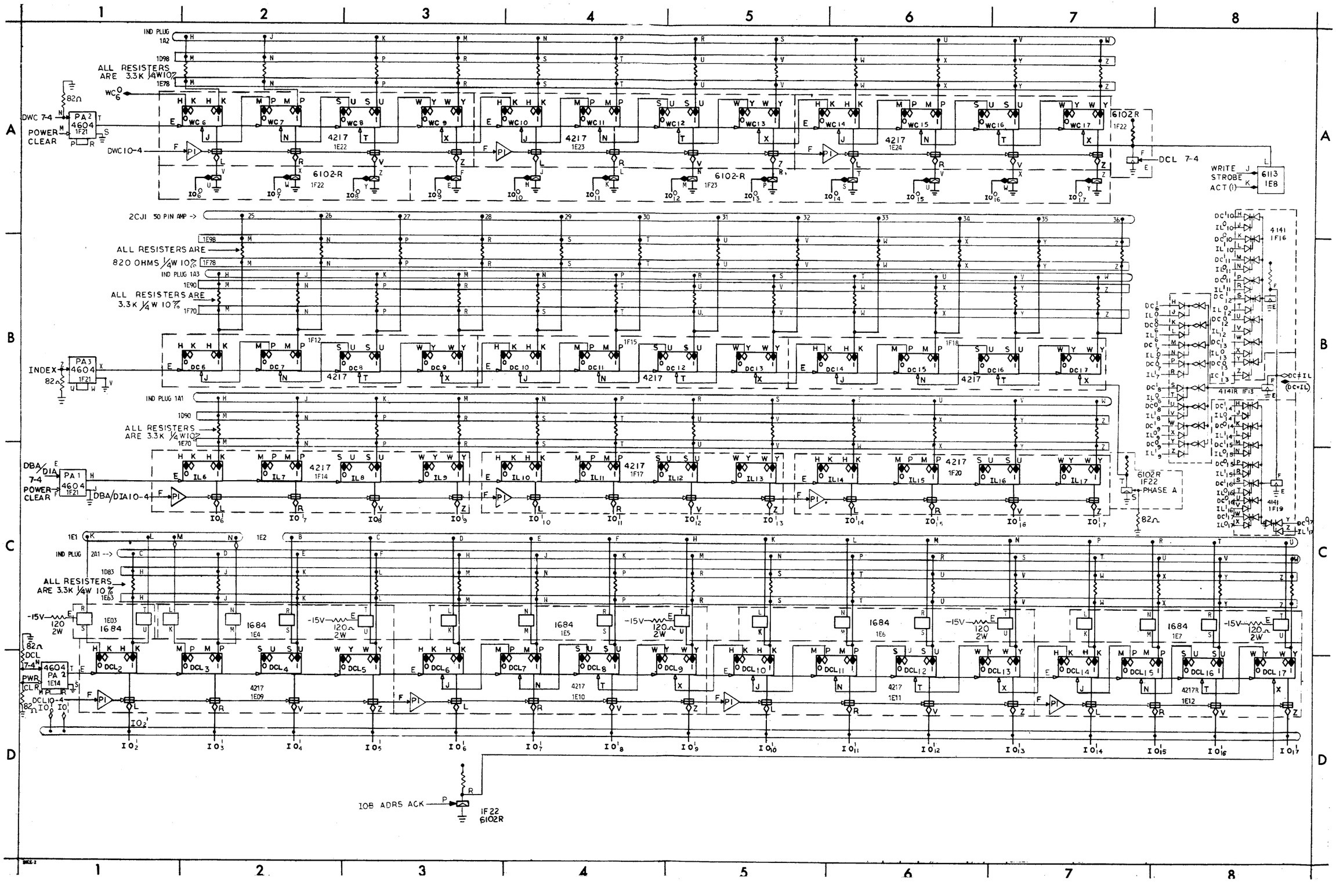
6102R 1F8

4217 1E19

Core Location, Drum Counter, Initial Location and Word

Counter BS-D-23-0-6

A3-35


1
2
3
4
5
6
7
8
A
B
C
D
IND PLUG 1A2
1D98
1E78
ALL RESISTERS ARE 3.3K 1/4W 10%
WC 6
82Ω
DWC 7-4
POWER CLEAR
PA2 4604 1F21
DWC 10-4
WC 6
WC 7
WC 8
WC 9
WC 10
WC 11
WC 12
WC 13
WC 14
WC 15
WC 16
WC 17
4217 1E22
4217 1E23
4217 1E24
6102-R 1F22
6102-R 1F23
6102R 1F22
DCL 7-4
WRITE STROBE ACT (I)
6113 1E8
2CJI 50 PIN AMP ->
1E98
ALL RESISTERS ARE 820 OHMS 1/4W 10%
1F78
IND PLUG 1A3
1E90
ALL RESISTERS ARE 3.3K 1/4W 10%
1F70
INDEX
PA3 4604 1F21
82Ω
DC 6
DC 7
DC 8
DC 9
DC 10
DC 11
DC 12
DC 13
DC 14
DC 15
DC 16
DC 17
4217 1F12
4217 1F15
4217 1F18
IND PLUG 1A1
1D90
1E70
ALL RESISTERS ARE 3.3K 1/4W 10%
DBA/DIA 7-4
POWER CLEAR
PA1 4604 1F21
DBA/DIA10-4
IL 6
IL 7
IL 8
IL 9
IL 10
IL 11
IL 12
IL 13
IL 14
IL 15
IL 16
IL 17
4217 1F14
4217 1F17
4217 1F20
6102R 1F22 PHASE A
82Ω
4141 1F16
4141R 1F13
4141 1F19
DC=IL
(DC≠IL)
1E1
1E2
IND PLUG 2A1 -->
1D83
1E63
ALL RESISTERS ARE 3.3K 1/4W 10%
-15V
120 2W
1E03 1684
1684 1E4
1684 1E5
1684 1E6
1684 1E7
DCL 2
DCL 3
DCL 4
DCL 5
DCL 6
DCL 7
DCL 8
DCL 9
DCL 10
DCL 11
DCL 12
DCL 13
DCL 14
DCL 15
DCL 16
DCL 17
82Ω
DCL 7-4
PWR CLR
PA 2 4604 1E14
DCL10-4
4217 1E09
4217 1E10
4217 1E11
4217R 1E12
IOB ADRS ACK
1F22 6102R

JACK [X] PLUG [ ] FEMALE [X] MALE [ ]	LOCATION, LENGTH, ROUTE 2CJ6

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED TWP	2B 8 H	1	RB 0	RED	2B20H	26	RB 12
GRN	2B 8 F	2	RB 0	GRN	20F	27	RB 12
RED	9 H	3	1	RED	21H	28	13
GRN	9 F	4	1	GRN	21F	29	13
RED	10H	5	2	RED	22H	30	14
GRN	10F	6	2	GRN	22F	31	14
RED	11H	7	3	RED	23H	32	15
GRN	11F	8	3	GRN	23F	33	15
RED	12H	9	4	RED	24H	34	16
GRN	12F	10	4	GRN	24F	35	16
RED	13H	11	5	RED	2B25H	36	RB 17
GRN	13F	12	5	GRN	2B25F	37	RB 17
RED	14H	13	6			38	
GRN	14F	14	6	RED	2B7H	39	RB_P
RED	15H	15	7	GRN	2B7F	40	RB_P
GRN	15F	16	7			41	
RED	16H	17	8	BLK	2B5D	42	CLOCK SHIELD
GRN	16F	18	8	RED	2B6H	43	INDEX START
RED	17H	19	9	BLK	2B6E	44	INDEX C TAP
GRN	17F	20	9	GRN	2B6F	45	INDEX FINISH
		21		BLK	2B6D	46	SHIELD
RED	18H	22	10	RED	2B5H	47	CLOCK START
GRN	18F	23	10	BLK	2B5E	48	CLOCK C TAP
RED	2B 19H	24	RB 11	GRN	2B5F	49	CLOCK FINISH
GRN	2B 19F	25	RB 11	BLK	2B CHASSIS	50	GND

Reader Output from Drum Housing (2CJ6) CL-A-23-0-13

JACK [x] PLUG [ ] FEMALE [x] MALE [ ]	LOCATION, LENGTH, ROUTE 2CJ4

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
BLACK	1C10W	1	FSB 0	BLACK	1D19W	26	FSB 31
	1C11W	2	1		1D20W	27	32
	1C12W	3	2		1D21W	28	33
	1C13W	4	3		1D22W	29	34
	1C14W	5	4		1D23W	30	35
	1C15W	6	5		1D24W	31	36
	1C16W	7	6	BLACK	1D25W	32	FSB 37
	1C17W	8	7			33	
	1C18W	9	10			34	
	1C19W	10	11			35	
	1C20W	11	12			36	
	1C21W	12	13			37	
	1C22W	13	14			38	
	1C23W	14	15			39	
	1C24W	15	16			40	
	1C25W	16	17			41	
	1D10W	17	20			42	
	1D11W	18	21			43	
	1D12W	19	22			44	
	1D13W	20	23			45	
	1D14W	21	24			46	
	1D15W	22	25			47	
	1D16W	23	26			48	
	1D17W	24	27			49	
BLACK	1D18W	25	FSB 30	BLACK	GND 1C CHASSIS	50	GROUND

Field Select Input to Drum Housing (2CJ4) CL-A-23-0-14

JACK [X] PLUG [ ] FEMALE [X] MALE [ ]	LOCATION, LENGTH, ROUTE 2CJ3

COLOR	PIN	PIN	NAME	COLOR	PIN	PIN	NAME
RED	1B3R	1	WB0	RED	1B20R	26	WB12
GRN	1B3K	2	WB0	GRN	1B20K	27	WB12
RED	1B4R	3	WB1	RED	1B21R	28	WB13
GRN	1B4K	4	WB1	GRN	1B21K	29	WB13
RED	1B5R	5	WB2	RED	1B22R	30	WB14
GRN	1B5K	6	WB2	GRN	1B22K	31	WB14
RED	1B6R	7	WB3	RED	1B23R	32	WB15
GRN	1B6K	8	WB3	GRN	1B23K	33	WB15
RED	1B7R	9	WB4	RED	1B24R	34	WB16
GRN	1B7K	10	WB4	GRN	1B24K	35	WB16
RED	1B8R	11	WB5	RED	1B25R	36	WB17
GRN	1B8K	12	WB5	GRN	1B25K	37	WB17
RED	1B9R	13	WB6			38	
GRN	1B9K	14	WB6	RED	1B2R	39	WBP
RED	1B10R	15	WB7	GRN	1B2K	40	WBP
GRN	1B10K	16	WB7			41	
RED	1B11R	17	WB8			42	
GRN	1B11K	18	WB8			43	
RED	1B17R	19	WB9			44	
GRN	1B17K	20	WB9			45	
		21				46	
RED	1B18R	22	WB10			47	
GRN	1B18K	23	WB10			48	
RED	1B19R	24	WB11			49	
GRN	1B19K	25	WB11	BLK	GND 1B CHASSIS	50	GND

Writer Input to Drum Housing (2CJ3) CL-A-23-0-15

JACK [X] PLUG [ ] FEMALE [X] MALE [ ]	LOCATION, LENGTH, ROUTE 2CJ1

COLOR	PIN	PIN	NAME TO	COLOR	PIN	PIN	NAME
WHITE	1E17L	1	IO 0 DRUM	WHITE	1E98N	26	DC 7 OUT
	1E17R	2	IO 1		P	27	DC 8
	1E19L	3	2		R	28	DC 9
	1E19R	4	3		S	29	DC 10
	1E19V	5	4		T	30	DC 11
	1E19Z	6	5		U	31	DC 12
	1F22V	7	6		V	32	DC 13
	1F22W	8	7		W	33	DC 14
	1F22Y	9	8		X	34	DC 15
	1F23E	10	9		Y	35	DC 16
	1F23H	11	10		1E98Z	36	DC 17
	1F23K	12	11	GRY/TWP	1E14V	37	DC→IO OUT
	1F23M	13	12	" "	1F4S	38	SBS RETURN
	1F23P	14	13	" "	1F21E	39	DIA 7-4 IN
	1F23S	15	14	" "	1E19F	40	DIA 10-4
	1F23U	16	15	" "	1F21N	41	DWC 7-4
	1F23W	17	16 TO	" "	1E24F	42	DWC 10-4
	1F23Y	18	IO 17 DRUM	" "	1F22E	43	DCL 7-4
	1E98E	19	ERROR STATUS	" "	1E12F	44	DCL 10-4
	1E98F	20	PAR ER OUT	" "	1F9W	45	DRA 7-4
	1E98H	21	TR. ER OUT	" "	1F9Y	46	DBA 7-4 IN
	1E98J	22	BUSY OUT	GREEN	2B PWR TAB	47	MC÷10
		23		BRN TWP	FILTER 1	48	REMOTE ON
		24		WHT TWP	FILTER 2	49	REMOTE ON
WHITE	1E98M	25	DC 6 OUT	BLK	GND 2C CHASSIS	50	GND

PDP-1D Interface With Drum Housing (2CJ1) CL-A-23-0-16

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