

# CHARACTER GENERATOR

# **VA 38**

## **20 $\mu$ s CHARACTER GENERATOR INSTRUCTION MANUAL**

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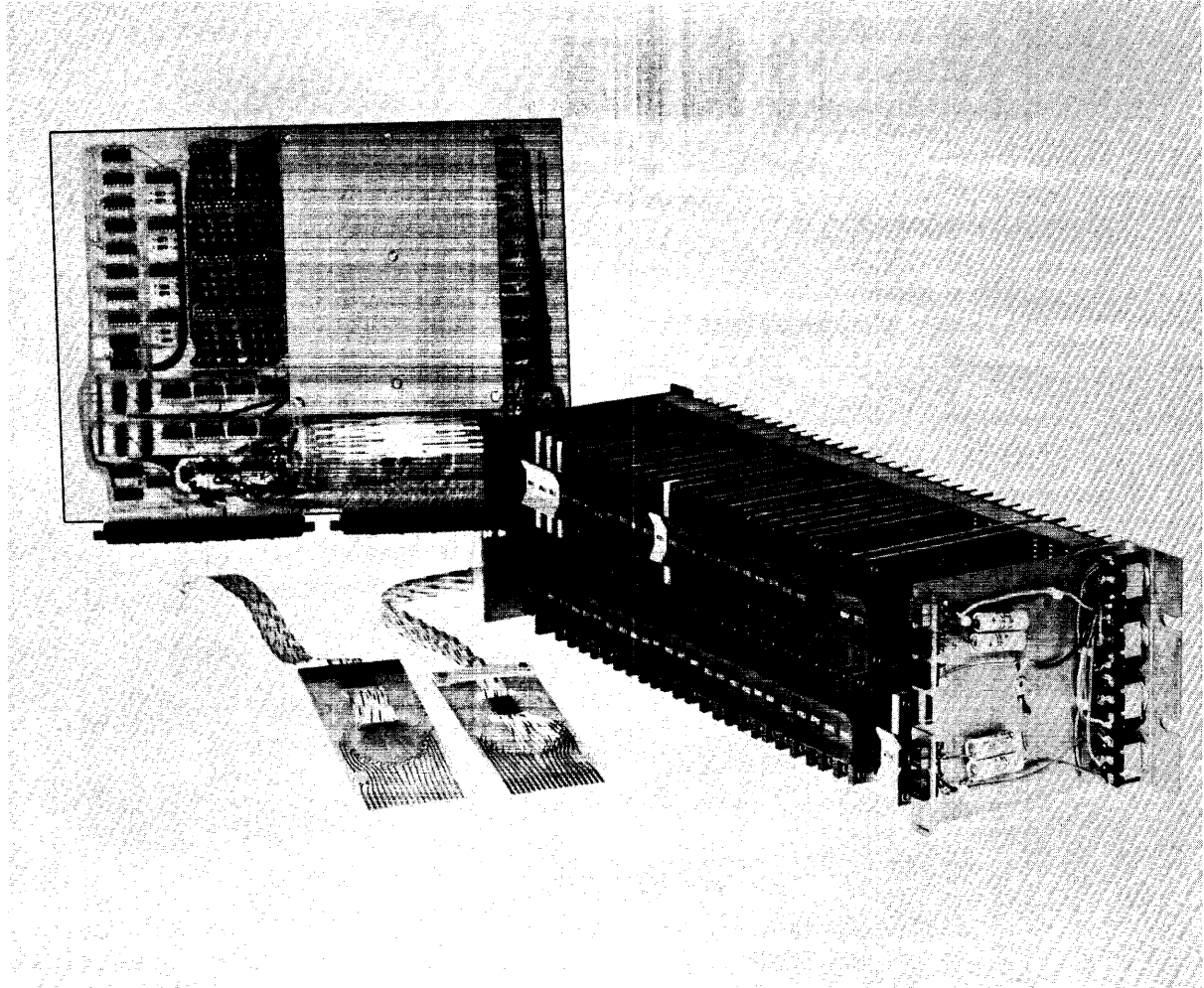
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VA38 20  $\mu$ s CHARACTER GENERATOR



VA38 20- $\mu$ s Character Generator

CHAPTER 1  
GENERAL INFORMATION

1.1 INTRODUCTION

The VA38 20  $\mu$ s Character Generator (frontispiece) is an option to the Type 338 or the Type 339 Programmed Buffered Display manufactured by Digital Equipment Corporation of Maynard, Massachusetts. The VA38-338 and VA39-339 systems evolve when the option is used with the 338 and 339 displays, respectively. The contents of this manual pertain to both cases. The option is used to generate ASCII (American Standard Code for Information Interchange) character information for the display. This document and the documents referenced herein provide the information necessary for installation, operation and maintenance of the option. The level of discussion assumes that the user is familiar with the display.

1.2 SPECIFICATIONS

The following specifications pertain to the VA38 20  $\mu$ s Character Generator.

1.2.1 Performance

Character format is fixed by the nature of the read-only memory and cannot be changed by the user. The character-generation-speed of 20  $\mu$ s per character allows the display of 1600 flicker-free ASCII characters.

1.2.2 Physical

The VA38 consists of a DEC standard 1943 Mounting Panel of FLIP-CHIP modules and a read-only memory. Both units mount in preassigned locations in the display as shown in Figure 2-1.

1.2.3 Power Requirements

The VA38 obtains all necessary operating power from the display with which it is used.

1.3 RELATED DOCUMENTATION

The documents listed in Table 1-1 contain information which supplements the information provided in this manual.

1.4 ENGINEERING DRAWING REFERENCES

VA38 control logic engineering drawings will be referenced by an abbreviated drawing number code. As an example, drawing D-BS-VA38-0-1, sheet 1, will be referenced as [VA-1(1)]. A complete VA38 control logic engineering drawing list is contained in Chapter 7 of this manual.

Table 1-1  
Reference Documents

Title	Document Number	Description
DIGITAL Logic Handbook	C-105	Specifications and descriptions of most FLIP-CHIP modules used in the VA38
338 Programmed Buffered Display Instruction Manual Volumes I and II	DEC-08-H6AA-D	Operation and programming information for the Type 338 Programmed Buffered Display
339 Programmed Buffered Display Instruction Manual	DEC-09-I6BA-D	Addendum to the 338 display manual, describing modifications of the 338 to the 339 display
Read-Only Memory System, Series SBS-1A to SBS-4B Instruction Manual		Operation and maintenance information for the read-only memory.





## CHAPTER 2 INSTALLATION

The VA38 installation should be attempted only by a DEC Field Engineer. Before proceeding with the following installation procedures, display operation should be checked by all display diagnostic programs.

VA38 installation consists of the procedures described in the following paragraphs, and requires the following equipment.

- Electric drill\*
- 1/4 in. bit\*
- 10-32 Rivnut gun
- Wire wrap gun
- Standard field service tool kit
- 10-32 x 3/4 in. machine screws (6)\*
- 10-32 external tooth lockwashers (6)\*
- 10-32 Rivnuts (6)\*
- B117 NAND/NOR Gate module (1)
- 4698 Intensity Amplifier module (1)
- Power jumpers
- Wire wrap wire
- R/C Terminator (0.01  $\mu$ Fd capacitor and 100 $\Omega$  resistor)
- MAINDEC-08-D8MA tape and write-up
- Copy of ECO 338-00003
- Copy of ECO 338-00004
- Set of 338 engineering drawings containing ECO 338-00004

### 2.1 MECHANICAL

The VA38 control logic and read-only memory mount in the relative display locations shown in Figure 2-1. The read-only memory is attached to the vertical supporting members of display bay 1, below the table assembly bracket. When properly installed, the memory proper should be near the back of bay 1 with the plated connector pins facing the front of the display.

Displays with serial numbers of 45 and greater have mounting holes for the VA38 read-only memory. The supplied screws and washers are used to secure the memory to the display. Displays with serial numbers

less than 45 do not have these holes. The memory must be positioned against the vertical supporting members of bay 1, the hole locations marked and drilled out with a 1/4 inch bit and the Rivnuts installed. The memory is then secured to the vertical supporting members with the supplied hardware.

The VA38 control logic modules are contained by a DEC Type 1943 Mounting Panel. Three mounting panel covers are located directly below the 338 Display CRT. To install the control logic, remove the middle panel cover and replace with the control logic. Secure the 1943 panel with the four screws that previously held the panel cover

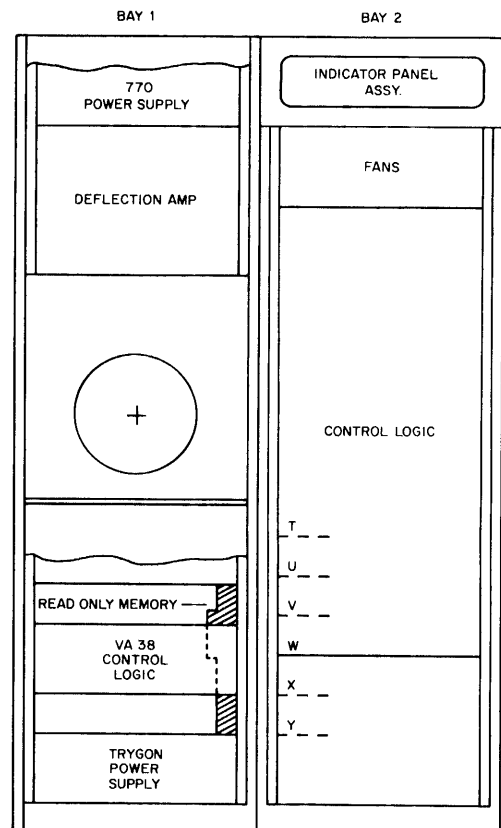


Figure 2-1 VA38-338 Installation Diagram

\*Required only for displays with serial numbers less than 45.

## 2.2 ELECTRICAL

Electrical installation of the VA38 involves connecting power wiring between the display and the control logic, and interface cables between the control logic, the read-only memory and the display.

The VA38 obtains operating and marginal power from the logic mounting panel above the display CRT. Power is supplied by jumper wires connected between the control logic and the mounting panel.

Four cables interface the VA38 control logic, the read-only memory and the 338 display. Figure 2-2 and Table 2-1 provide all necessary interface cabling information. It should be noted that the plated connector pins of the memory are arranged in two groups, P1 and P2, and are designated as such on the memory. When the memory is properly installed, P2 will be above P1. The 80-pin cable connectors can attach to the plated pins correctly or upside down. When correctly attached the connector end stamped "50-90" will face upward.

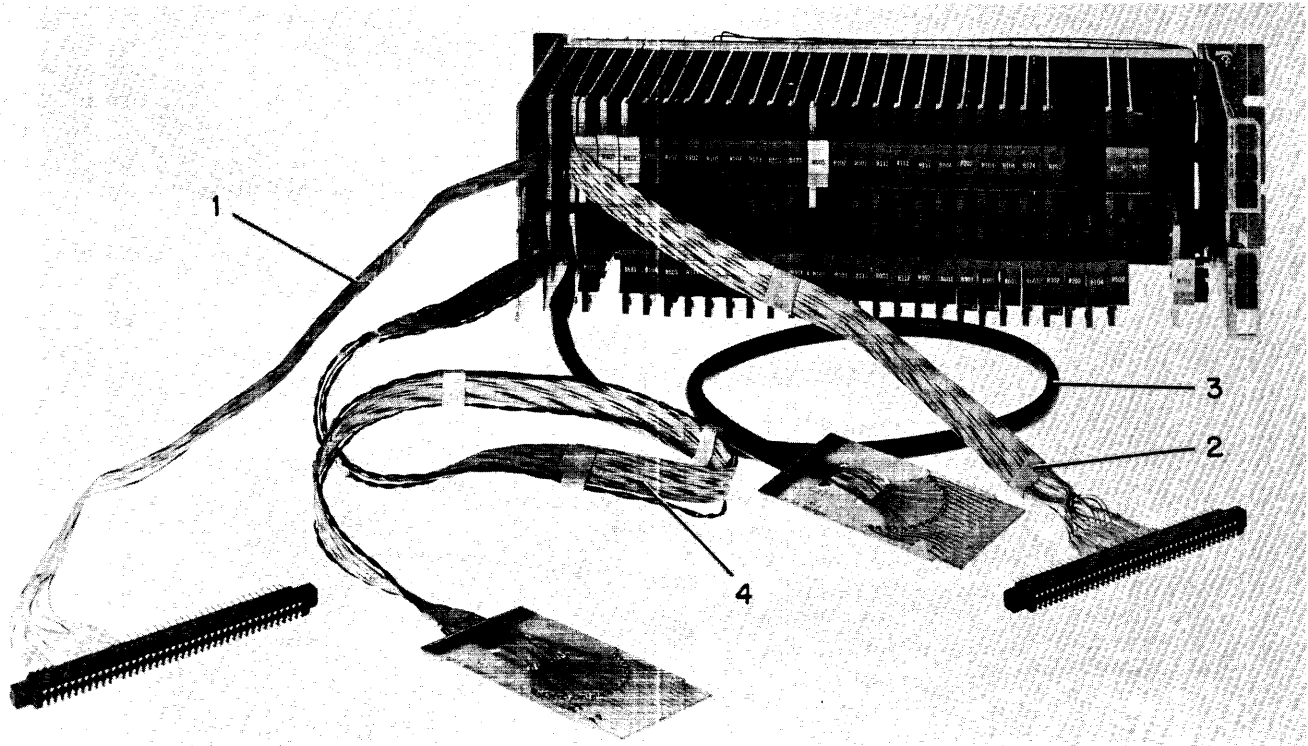


Figure 2-2 VA38 Cables

Table 2-1  
VA38-338 Cabling Information

No.	Location	From Type	Section	Location	To Type	Section	Engineering Drawings
1	A32	W023	CONTROL	P2	259-80-90-226	ROM	7005816-0-0
2	A31	W023	CONTROL	P1	259-80-90-226	ROM	7005815-0-0
3	B31	W023	CONTROL	L01	W023	338	
4	B32	W023	CONTROL	L02	W023	338	7005814-0-0

### 2.3 DISPLAY MODIFICATIONS

Incorporation of a VA38 20  $\mu$ s Character Generator into a 338 Programmed Buffered Display requires the modifications described in the following paragraphs.

a. The following Engineering Change Orders (ECO) must be executed. ECO 338-00004 which pertains only to the display should be incorporated first and checked by all 338 diagnostic programs. When installation proves correct, ECO 338-00003, which pertains only to the VA38/39, should be executed. The wire list for ECO 338-00004 is provided in Table 2-2; ECO 338-00003 is provided in Table 2-3. These wire lists should be used.

b. Two modules are also required for VA38 implementation. A B117 NAND/NOR Gate must be inserted in display location R26, and the 4688 Intensity Amplifier found in display location Z02 must be replaced by the supplied high-speed 4698 Intensity Amplifier which is described in Section 6.2.

Following installation of the 4698 module, the high voltage interlock switches, located at the back of both display bays, should be placed in the OFF position until the intensity time delay is set as described below.

c. Two display delays require changes: The Break Request delay, location S07V, must be increased to 500 ns; the Intensify Time delay, location M25F must be decreased from 300 ns to 100 ns.

Table 2-2  
Wire List for ECO 338-00004

Make All Deletions First					
Signal Name	From Pin	To Pin	Components	Add	Del .
INT 0 (0)	F05S	N02E			x
INT 1 (0)	F05T	N02F			x
INT 2 (0)	F05U	N02H			x
INT 0 (1)	P01C	F11P		x	
B INT 0 (1)	F11R	F11S		x	
B INT 0 (1)	F11R	F05S		x	
INT 1 (1)	P01D	F11U		x	
B INT 1 (1)	F11V	F05T		x	
B INT 1 (1)	E10S	F05T		x	
INT 2 (1)	P01E	E10T		x	
B INT 2 (1)	E10U	E10V		x	
B INT 2 (1)	E10V	F05U		x	
GND 11	F11C	H11C			x
GND 11	F11C	F11N		x	
GND 11	F11N	F11T		x	
GND 11	F11T	H11C		x	

Table 2-3  
Wire List for ECO 338-00003

Make All Deletions First					
Signal Name	From Pin	To Pin	Components	Add	Del .
	P25D		Delete from Run		x
	L30F	GND			x
	L01D	J08D		x	
	L01E	J08J		x	
	L01E	N17P		x	
	L01F	L12E		x	
	L01H	M07E		x	
	L01H	L12K		x	
	L01J	M04K		x	
	L01K	M05K		x	
	L01K	J12L		x	
	L01L	N13D		x	
	L01M	L07U		x	
	L07U	L09H		x	
	L09H	P17V		x	
	P17V	S03N		x	
	L01N	L18T		x	
	L01P	L29D		x	
	L01R	N02L		x	
	L01S	M30D		x	
	L01T	N15E		x	
	L01U	N27P		x	
	L01V	GND		x	
	L02D	H23F		x	
	L02E	GND		x	
	L02F	F14T		x	
	L02H	H24T		x	
	L02J	L25P		x	
	L02K	L26T		x	
	L02L	L10E		x	
	L10E	J07H		x	

Table 2-3 (Cont)  
Wire List for ECO 338-00003

Signal Name	From Pin	To Pin	Components	Add	Del .
	L02M	N09K		x	
	L02N	L21F		x	
	L21F	M21E		x	
	L02P	N31T		x	
	L02R	S14P		x	
	L02S	N28N		x	
	L02T	H11F		x	
	L02U	P02H		x	
	L02V	GND		x	
	R26D	J21H		x	
	R26E	J09S		x	
	R26F	J21P		x	
	R26H	J29K		x	
	R26J	J29R		x	
	R26K	J23S		x	
	R26L	P25H		x	
	R26L	R26V		x	
	R26V	R27J		x	
	R26M	GND		x	
	R26N	K31R		x	
	R26P	K09N		x	
	R26R	J26K		x	
	R26S	K32R		x	
	R26T	J30D		x	
	R26U	J25S		x	
	R25R	P25K		x	
	P25K	P25J		x	
	R25S	N10D		x	
	N10D	L30F		x	
	L30F	L07T		x	
	R25V	R25U		x	

Table 2-3 (Cont)  
Wire List for ECO 338-00003

Signal Name	From Pin	To Pin	Components	Add	Del.
	R25U	L09F		x	
	L09F	L09E		x	
	R13U	L09D		x	
	S14S	S15F		x	
	S03P	S04M		x	
	P25D	K26U		x	
	N07T	N10H		x	
	N09L	N29K		x	
	L25M	L25S		x	
	L26U	L26V		x	
	L30P	GND		x	
	F05E	F14U		x	
	F14U	F14V		x	
	H18H	H24U		x	
	H24U	H24V		x	

Add B117 Module in Location R26 in the 338 Logic

CHAPTER 3  
OPERATION AND PROGRAMMING

The VA38 is completely under the control of the display with which it is used. No controls or indicators are found on the VA38.

3.1 PROGRAMMING

The character generator is accessed by a mode instruction containing an enter mode 7, enter data state command 1171. Mode 7 is reserved for the character generator. The words read from PDP-8 memory are de-

coded as two characters per word. Special character ESC (escape), described in Section 4.11, allows the display to leave the data state and enter the control state. The next word in the display file is interpreted as a control word.

The sample program below illustrates the program simplicity of the VA38. Figure 3-1 illustrates the five character sets (320 characters) produced by such a program.

				/FIVE CHARACTER SETS
0200	7200	BEGIN,	CLA	/PROGRAM START
0201	1215		TAD PTR	
0202	6135		SPDP	/SET THE PUSH DOWN POINTER
0203	7200		CLA	
0204	1216		TAD IC	
0205	6145		SIC	/SET THE INITIAL CONDITIONS
0206	7200		CLA	
0207	1217		TAD BF	
0210	6155		LBF	/LOAD THE BREAK FIELD
0211	7200		CLA	
0212	1220		TAD SA	
0213	6165		INIT	/INITIALIZE THE DISPLAY
0214	5214		JMP	
0215	4000	PTR,	4000	
0216	0004	IC,	0004	
0217	4000	BF,	4000	
0220	0221	SA,	FILE	
0221	0517	FILE,	SC1 INT7	/PARAMETER WORD
0222	1107		POINT EDS	/POINT WORD
0223	1700		1700	
0224	4000		4000	
0225	2010		PJMP	/JUMP TO SUBROUTINE
0226	0241		CHAR	/THAT CONTAINS THE
0227	2010		PJMP	/CHARACTER SET
0230	0241		CHAR	
0231	2010		PJMP	
0232	0241		CHAR	
0233	2010		PJMP	
0234	0241		CHAR	
0235	2010		PJMP	
0236	0241		CHAR	
0237	2000		DJMP	/JUMP TO START OF
0240	0221		FILE	/THE DISPLAY FILE



0241	1171	CHAR,	CHARM EDS	/MODE COMMAND TO
0242	0001		0001	/ENTER CHARACTER
0243	0203		0203	/GENERATOR
0244	0405		0405	
0245	0607		0607	
0246	1011		1011	/TWO CHARACTER CODES PER WORD
0247	1213		1213	
0250	1415		1415	
0251	1617		1617	
0252	2021		2021	
0253	2223		2223	
0254	2425		2425	
0255	2627		2627	
0256	3031		3031	
0257	3233		3233	
0260	3435		3435	
0261	3637		3637	
0262	4041		4041	
0263	4243		4243	
0264	4750		4750	
0265	5152		5152	
0266	5354		5354	
0267	5556		5556	
0270	5760		5760	
0271	6162		6162	
0272	6364		6364	
0273	6566		6566	
0274	6770		6770	
0275	7172		7172	
0276	7374		7374	
0277	7576		7576	
0300	7700		7700	
0301	4445		4445	/CARRIAGE RETURN, LINE FEED
0302	4600		4600	/ESCAPE CHARACTER
0303	3000		POP	/RETURN FROM SUBROUTINE

SPDP=6135  
 SIC=6145  
 LBF=6155  
 INIT=6165  
 SC1=0500  
 INT7=0017  
 POINT=1106  
 EDS=1001  
 PJMP=2010  
 DJMP=2000  
 CHARM=1170  
 POP=3000

BEGIN	0200
BF	0217
CHAR	0241
CHARM	1170
DJMP	2000
EDS	1001
FILE	0221

IC	0216
INIT	6165
INT7	0017
LBF	6155
PJMP	2010
POINT	1106
POP	3000
PTR	0215
SA	0220
SC1	0500
SIC	6145
SPDP	6135

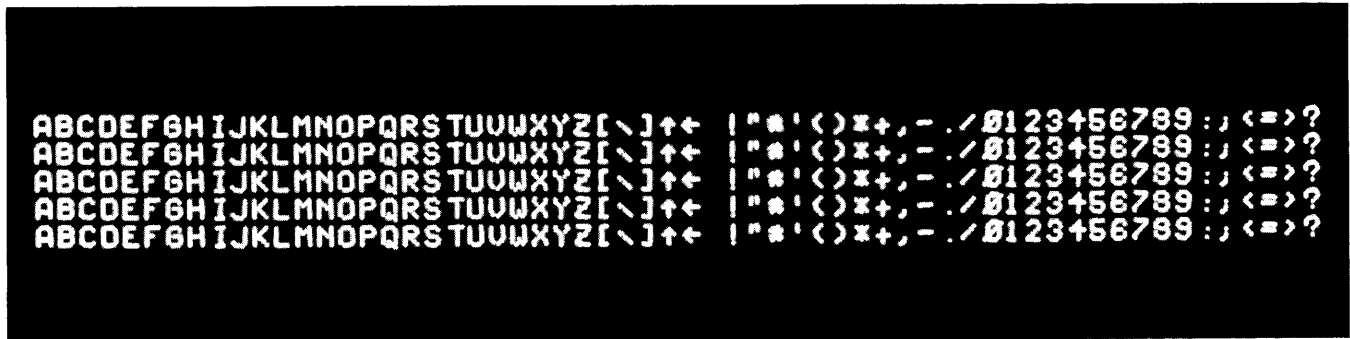


Figure 3-1 Sample Program Characters



CHAPTER 4  
PRINCIPLES OF OPERATION

4.1 GENERAL

The VA38 20  $\mu$ s Character Generator consists of control logic and a read-only memory. Figure 4-1 illustrates the relationship between these units and the 338 Programmed Buffered Display with which it is used.

Basically, characters are generated from a series of 6-bit character words stored in the read-only memory (ROM). To initiate generation of a character, the ASCII code for the character desired is applied to the VA38 control logic. It is combined with an internally produced 4-bit word to provide the 10-bit address re-

quired by the ROM. Under control of the 338 display, the character generator control logic produces a START CYCLE pulse to read a character word out of the ROM and into the ROM output data register. The word is then jam transferred into the VA38 control logic where it is decoded. While this character word is being incremented in preparation for the next word of the character, the current word provides character information for the display. After this word has been completely decoded, an XFER INIT pulse is produced again and the 6-bit word at the incremented address is jam transferred into the control logic. The address is again incremented during this time. This chain continues until the end of the character is sensed.

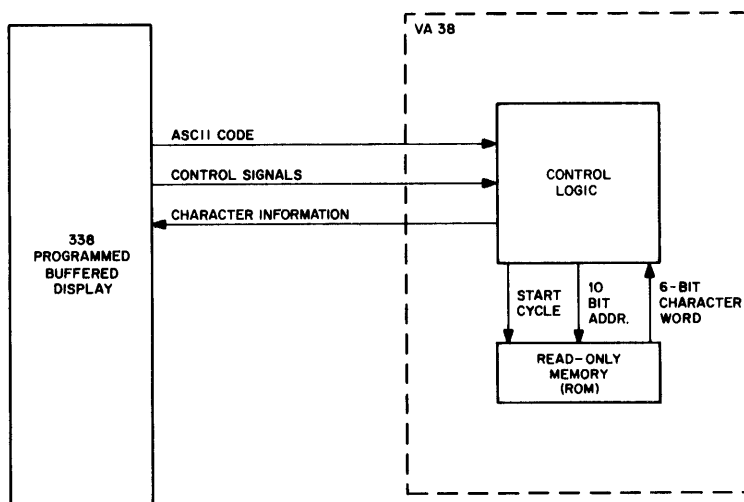


Figure 4-1 VA38 - 338 System Block Diagram

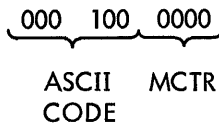
4.2 ASCII CHARACTER SET

Figure 4-2, ASCII Character Set, provides the character code, ROM address and character words for all ASCII characters capable of being generated by the VA38. Before proceeding, it should be noted that the ROM requires a 10-bit address consisting of 6 high-order bits from the ASCII character code and 4 low-order bits from the internal VA38 MCTR (memory coun-

ter). The high-order portion of the address remains fixed throughout a given character while the MCTR is incremented and the low-order portion changes.

The character "D" will serve as an example in explaining the use of the table. D has the ASCII code of 04. The code comprises 6 bits of the 10-bit address. The remaining 4 bits are obtained from the content of the MCTR which is cleared at the beginning of a character.

Thus the initial 10-bit ROM address will be



Converted to octal, the address becomes 100g. Character word 72g is obtained from this address. The word is jam transferred into the VA38 CH REGISTER, from which it is decoded, as explained in Section 4.6, CH Register, and Section 4.7 Character Information Utilization.

While the current word is being decoded, the MCTR is incremented and the address becomes 101. This cycle continues until the end of the character is sensed via 06. The MCTR is then cleared.

A maximum of 64 ASCII characters can be produced by the VA38. Of these, three are termed "special",

they are CR (carriage return), LF (line feed) and ESC (escape) and they replace \$, %, and &, respectively.

The usual characters will be termed common and will be explained as a group since the operations they initiate are basically the same. The special characters will be explained separately.

### 4.3 COMMON CHARACTER GENERATION

Section 4.4 and 4.5, Common Character Signal Flow and Character End Signal Flow, respectively, illustrate the timing chain for all common characters. Section 4.4 illustrates the operations which serve to condition the VA38 control logic, address the read-only memory and decode the character words from memory. Reference should also be made to Section 4.6 and 4.7 as they contain information regarding specific character word decoding and resultant functions.

Section 4.5 illustrates the operations that result when the completion of the character is sensed.

Code	Character	Code	Character	
00	@	40	SPC	
01	A	41	!	
02	B	42	"	
03	C	43	#	
04	D	44	\$ CR	Special characters include control words which may be decoded to implement the functions: CR LF ESCAPE (The LF word forces a reference to R/O MEM LOC 0014. This section contains coding for execution of LF)
05	E	45	% LF	
06	F	46	& ESC	
07	G	47	'	
10	H	50	(	
11	I	51	)	
12	J	52	*	
13	K	53	+	
14	L	54	,	
15	M	55	-	
16	N	56	.	
17	O	57	/	
20	P	60	0	
21	Q	61	1	
22	R	62	2	
23	S	63	3	
24	T	64	4	
25	U	65	5	
26	V	66	6	
27	W	67	7	
30	X	70	8	
31	Y	71	9	
32	Z	72	:	
33	[	73	;	
34	\	74	<	
35	]	75	=	
36	†	76	>	
37	+	77	?	

Figure 4-2 VA38 ASCII Character Set

	0	4	10	14	20	24	30	34	40	44	50	54	60	64	70	74
	0	100	200	300	400	500	600	700	1000	1100	1200	1300	1400	1500	1600	1700
Word																
00																
0	71	72	40	72	40	32	40	01	30	03	32	57	40	20	62	30
1	53	72	72	72	72	22	52	32	30	52	71	51	71	50	12	10
2	65	70	72	36	72	12	71	52	10	67	25	52	71	72	62	73
3	62	57	36	26	70	70	51	77	06	72	66	17	14	72	51	61
4	51	76	70	56	57	60	52	57	07	63	67	30	74	75	60	37
5	60	56	32	70	56	24	34	30	07	52	30	10	55	60	57	17
6	57	55	50	50	55	76	54	06	07	61	10	06	76	10	56	16
7	66	74	76	30	64	76	56	07	07	67	06	07	26	60	55	06
10	55	30	76	06	37	30	57	07	07	23	07	07	70	27	64	07
11	17	30	30	07	30	10	17	07	07	76	07	07	51	16	30	07
12	30	10	06	07	06	06	67	07	07	67	07	07	72	06	66	07
13	06	06	07	07	07	07	56	07	07	56	07	07	27	07	55	07
14	36	07	07	07	07	07	30	07	07	55	07	07	26	07	64	07
15	36	07	07	07	07	07	06	07	07	30	07	07	06	07	30	07
16	36	07	07	07	07	07	07	07	07	10	07	07	07	07	30	07
17	06	07	07	07	07	07	07	07	07	06	07	07	07	07	06	07
20	40	72	10	40	72	72	10	02	20	04	50	22	70	52	52	12
21	62	72	70	62	62	72	50	70	40	52	61	52	53	57	57	52
22	72	70	53	72	51	30	72	72	12	71	62	70	72	60	60	70
23	51	35	72	52	60	50	63	72	72	51	63	50	62	51	51	50
24	60	60	23	67	57	76	52	64	62	24	37	37	55	52	72	12
25	57	25	70	61	76	66	30	37	37	64	37	06	37	53	52	52
26	76	56	55	76	34	55	50	37	27	56	06	07	27	74	53	74
27	66	70	37	76	77	64	10	06	16	50	07	07	10	72	64	54
30	22	50	17	30	13	30	65	07	06	17	07	07	06	70	55	37
31	74	30	16	06	64	30	37	07	07	67	07	07	07	50	56	17
32	37	06	06	07	20	06	17	07	07	54	07	07	07	37	57	30
33	21	07	07	07	51	07	06	07	07	51	07	07	07	36	60	06
34	17	07	07	07	27	07	07	07	07	27	07	07	07	06	37	07
35	06	07	07	07	11	07	07	07	07	10	07	07	07	07	10	07
36	07	07	07	07	06	07	07	07	07	06	07	07	07	07	06	07
37	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07	07
40	40	40	52	40	40	51	52	20	32	05	20	20	40	72	20	71
41	62	72	57	62	62	53	71	40	51	62	72	50	71	70	50	63
42	72	72	60	72	72	72	51	72	62	61	62	30	51	11	22	37
43	52	70	51	52	52	52	52	62	10	52	26	10	52	52	52	17
44	70	50	72	77	70	30	74	65	50	53	63	06	53	53	37	17
45	57	35	62	50	57	50	54	21	66	55	27	07	64	64	10	10
46	56	40	27	72	56	76	26	67	37	56	61	07	55	55	06	06
47	55	50	36	36	55	56	57	37	17	17	25	07	36	56	07	07
50	64	37	17	76	64	65	10	06	06	77	65	07	26	36	07	07
51	30	20	06	30	77	30	50	07	07	14	21	07	70	16	07	07
52	66	06	07	06	30	20	25	07	07	64	67	07	50	70	07	07
53	55	07	07	07	06	06	55	07	07	21	17	07	30	51	07	07
54	64	07	07	07	07	07	70	07	07	50	20	07	06	52	07	07
55	30	07	07	07	07	07	50	07	07	27	06	07	07	27	07	07
56	30	07	07	07	07	07	30	07	07	10	07	07	07	10	07	07
57	06	07	07	07	07	07	06	07	07	06	07	07	07	06	07	07
60	72	72	40	72	52	72	00	30	71	31	17	52	52	40	57	32
61	62	62	72	62	57	72	70	73	63	53	10	71	57	52	51	62
62	51	51	72	51	60	30	24	61	76	62	72	51	60	71	52	51
63	60	60	30	60	51	50	72	25	54	37	64	37	51	51	12	60
64	57	57	50	57	52	76	72	70	12	27	20	26	52	52	52	57
65	35	25	75	76	53	66	60	60	52	16	62	06	53	74	37	56
66	15	14	77	56	64	55	37	27	21	06	26	07	54	54	20	65
67	57	70	30	55	53	53	26	16	67	07	60	07	13	37	06	16
70	60	66	06	64	52	52	17	06	54	07	27	07	53	37	07	56
71	51	55	07	30	51	15	06	07	16	07	10	07	51	10	07	30
72	30	64	07	30	60	56	07	07	66	07	06	07	60	06	07	20
73	16	30	07	06	57	30	07	07	51	07	07	07	57	07	07	06
74	06	30	07	07	37	30	07	07	27	07	07	07	56	07	07	07
75	07	06	07	07	26	06	07	07	10	07	07	07	37	07	07	07
76	07	07	07	07	06	07	07	07	06	07	07	07	16	07	07	07
77	07	07	07	07	07	07	07	07	07	07	07	07	06	07	07	07

Figure 4-2 VA38 ASCII Character Set (Cont)

#### 4.4 COMMON CHARACTER SIGNAL FLOW

Prior to character generation, GENERAL CLR conditions the VA38 control logic. The pulse is the OR condition of CHARM or B PWR CLR or IOT 164. CHARM is produced when the display enters the character mode. B PWR CLR is produced when power is first applied to the system or when the computer START key is actuated. IOT 164, Resume After Stop Code, is usually executed following the raising of an internal display stop flag.

Following logic conditioning operations, CHARM will be produced when the display enters the character mode. The level conditions an internal VA38 DCD gate which is strobed by DY LEFT DATA AVAIL. The result is CODE AVAIL which initiates character generation.

CODE AVAIL is gated with CHAR DONE (1) to produce START CYCLE. This pulse conditions the read-only memory (ROM) sense amplifiers and output data register and also allows the 10-bit memory address access to the ROM address decoding circuitry.

START CYCLE, delayed 400 ns, is READ DELAY. The delay allows sufficient time to read the 6-bit character word of the current ROM address out of the rope memory and into the output data register.

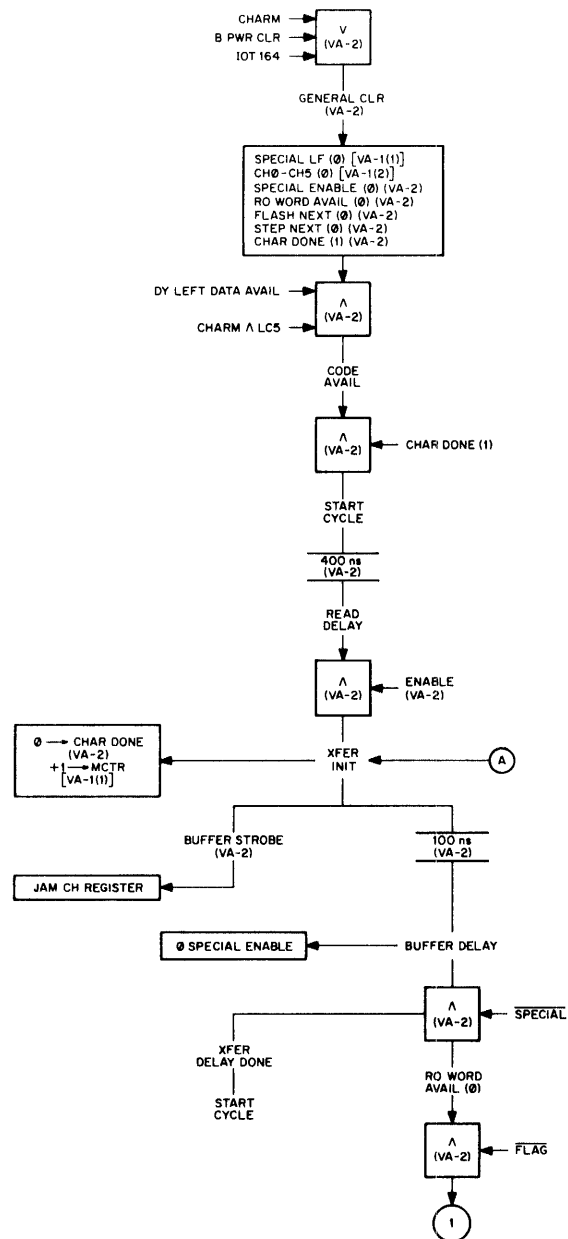
Delay termination results in a -3V → 0V transition which strobes a DCD gate conditioned by ENABLE which is the result of CHAR DONE (1). The result, XFER INIT, clears CHAR DONE and increments the MCTR.

XFER INIT triggers a 100 ns delay to produce BUFFER STROBE (100 ns, -3V level) and BUFFER DELAY at the termination of the delay. BUFFER DELAY allows the current 6-bit character word (bit 1 through bit 6), held in the ROM output data register, to be jam transferred into the VA38 CH REGISTER.

The contents of the CH REGISTER are applied to a binary to octal decoder where a SPECIAL of a SPECIAL condition is determined. All common character words will produce a SPECIAL condition because  $CH0 \wedge CH1 \wedge CH2 \neq 0$ . The decoder will be disabled and no LCn levels will be produced. BUFFER DELAY will not produce any Cn pulses.

NOTE: n is 0 through 7

BUFFER DELAY and SPECIAL produce XFER DELAY DONE which, in turn, produces a second START CYCLE pulse. This enables the 6-bit character word of the incremented ROM address to be read out of the rope memory and into the output data register. ENABLE is not present because of CHAR DONE (0), therefore no further action is taken on this character word.



If  $\overline{\text{CH1}}$  and  $\overline{\text{CH2}} \neq 0$ , producing  $\overline{\text{COUNT ZERO}}$ ,  $\text{STEP TIME}$  will generate  $\text{STEP}$  to complement  $\text{CH2}$ .  $\text{STEP TIME}$  also sets the  $\text{FLASH NEXT}$  flip-flop and triggers a 400 ns delay to produce  $\text{STEP TIME DELAY}$  (400 ns, 0V level) which complements  $\text{CH1}$ . Thus, the number-of-moves counter consisting of  $\text{CH1}$  and  $\text{CH2}$  is decremented by one.

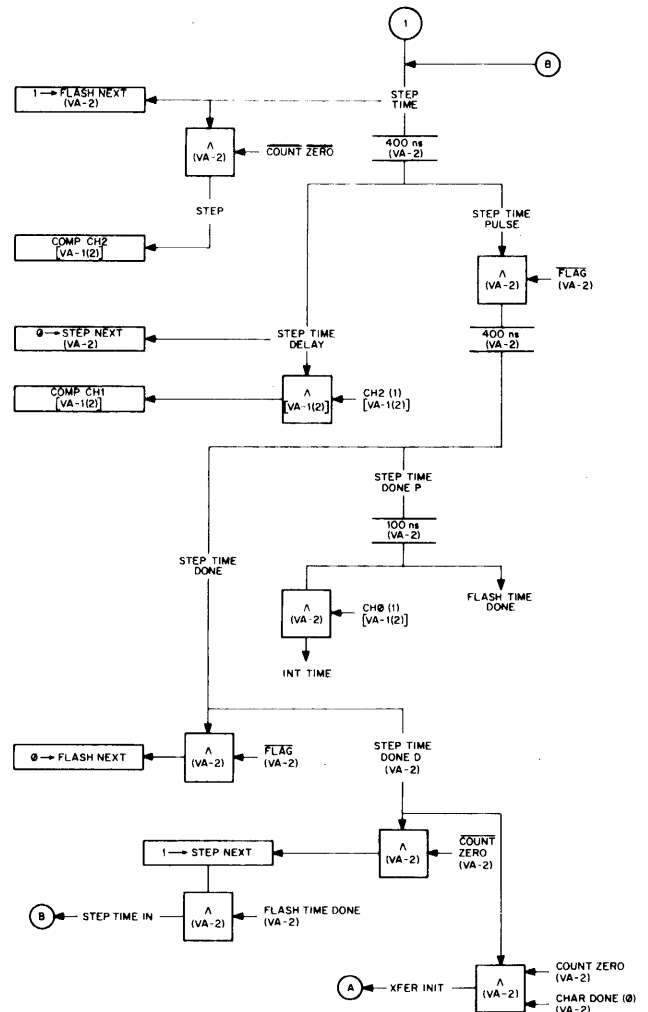
If  $\text{CH1}$  and  $\text{CH2} \neq 0$ , producing  $\overline{\text{COUNT ZERO}}$ ,  $\text{STEP TIME}$  will generate  $\text{STEP}$  to complement  $\text{CH2}$ .  $\text{STEP TIME}$  also sets the  $\text{FLASH NEXT}$  flip-flop and triggers a 400 ns delay to produce  $\text{STEP TIME DELAY}$  (400 ns, 0V level) which complements  $\text{CH1}$ . Thus, the number-of-moves counter consisting of  $\text{CH1}$  and  $\text{CH2}$  is decremented by one.

$\text{STEP TIME DELAY}$  clears the  $\text{STEP NEXT}$  flip-flop.  $\text{STEP TIME PULSE}$  occurs 400 ns after  $\text{STEP TIME}$  and is gated with  $\text{FLAG}$  to trigger a second 400 ns delay.

If  $\text{COUNT ZERO}$  is true, indicating that the current character word is completed,  $\text{XFER INIT}$  will be produced via  $\text{COUNT ZERO} \wedge \text{CHAR DONE (0)} \wedge \text{STEP TIME DONE D}$ . If  $\text{COUNT ZERO}$  is true, indicating that the current word has not been completed, the  $\text{STEP NEXT}$  flip-flop will be set and the word will be cycled through until  $\text{COUNT ZERO}$  is true. Assuming the end of the character is not sensed, a new 6-bit character word will be jam transferred into the  $\text{CH REGISTER}$ .

$\text{STEP TIME DONE-P}$  is produced with  $\text{STEP TIME DONE}$ . This pulse triggers a 100 ns intensity delay. If  $\text{CH0}$ , the intensity bit, is in the 1 state,  $\text{INT TIME}$  will be produced for 100 ns. This -3V level is utilized by the display intensity circuitry. Termination of the delay results in the production of  $\text{FLASH TIME DONE}$ .  $\text{FLASH TIME DONE}$  and  $\text{STEP NEXT (1)}$  produce  $\text{STEP TIME}$  which, in turn, is gated with  $\text{COUNT ZERO}$  to produce  $\text{STEP}$ .

The 338 display is provided with three types of character information for character display. Namely, intensity information, specified by  $\text{INT TIME}$ , number of moves, specified by the number of times a given character word is cycled through and direction of moves, described in Section 4.7.



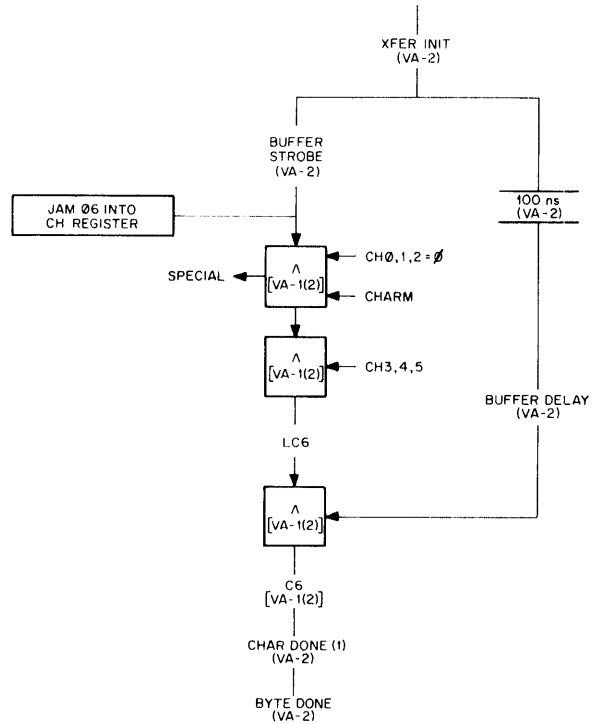


#### 4.5 END CHARACTER SIGNAL FLOW

Referring to Figure 4-2, ASCII Character Set, it is observed that all characters terminate with character word 06. When this word is sensed, logic operations result which signal the display that the current character has been fully decoded.

Completion of the character word preceding 06 produces an XFER INIT pulse to produce BUFFER STROBE. BUFFER STROBE jam transfers 06 from the ROM output data register into the VA38 CH REGISTER.

CH0, CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC6 to be produced from the remaining CH bits. LC6 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C6. C6, in turn, sets the CHAR DONE flip-flop to produce BYTE DONE. This signals the display that another ASCII character code may be sent to the VA38 control logic.



#### 4.6 CH REGISTER

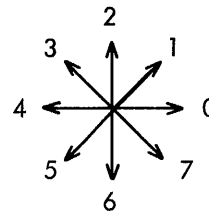
The VA38 CH REGISTER is essentially a storage register from which character words are decoded. The register format is as follows:

CH 0	CH 1	CH 2	CH 3	CH 4	CH 5
Inten-sity	Number of Moves		Direction		

CH0 and VA38 control signals are used to generate INT TIME which is used by the display to intensify a point.

A maximum of three moves can be specified by a single character word. The initial content of CH1 and CH2 dictates the number of times the current word will be cycled through.

Any of eight directions can be specified via the content of CH3 - CH5. The content/direction relationship is as shown:



#### 4.7 CHARACTER INFORMATION UTILIZATION

As previously stated, INT TIME is sent to the display to intensify the dot. Number-of-moves information is sent to the display via CX (COUNT X) and CY (COUNT Y) pulses. These pulses count the X- and Y-position registers. Direction information is applied to the display via CHARM LEFT and CHARM DOWN. Combinations of CHARM LEFT, CHARM DOWN, CX and CY are illustrated in Table 4-1.

Table 4-1  
Direction Information

↑	CY	CHARM DOWN (0V)
↓	CY	CHARM DOWN (-3V)
→	CX	CHARM LEFT (0V)
←	CX	CHARM LEFT (03V)
↗	CX, CY	CHARM LEFT (0V) and CHARM DOWN (0V)
↘	CX, CY	CHARM LEFT (-3V) and CHARM DOWN (-3V)
↖	CX, CY	CHARM LEFT (-3V) and CHARM DOWN (0V)
↙	CX, CY	CHARM LEFT (0V) and CHARM DOWN (-3V)

#### 4.8 SPECIAL CHARACTER GENERATION

As previously stated, the VA38 character repertoire contains a number of SPECIAL characters. Namely:

ASCII Character	SPECIAL Character
\$	CR (Carriage Return)
%	LF (Line Feed)
&	ESC (Escape)

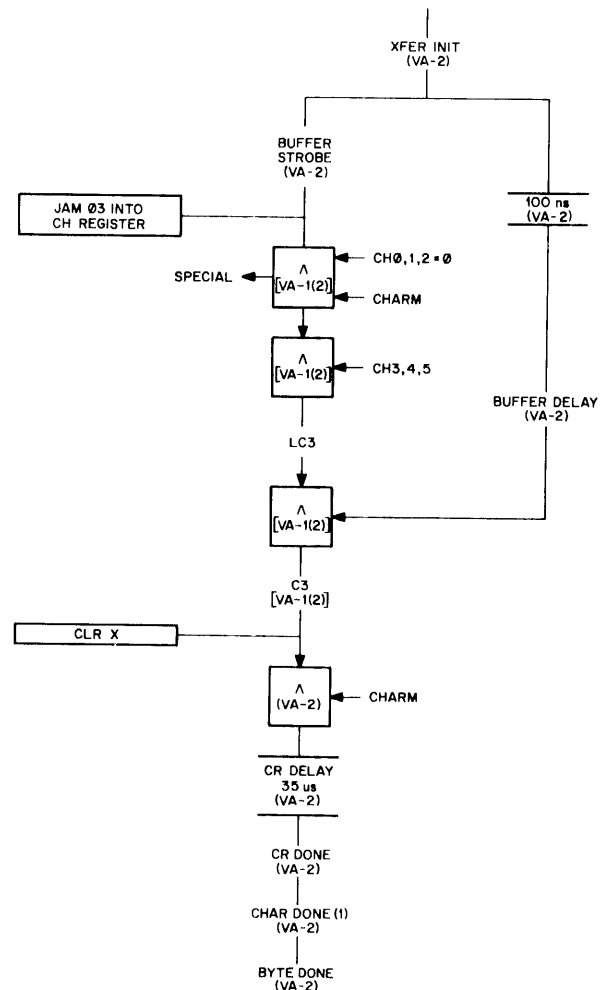
#### 4.9 CR (CARRIAGE RETURN) SIGNAL FLOW

CR is a SPECIAL character which move the dot and further information to be displayed to the left edge of the display CRT.

When CR (octal code 44) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC3 to be produced from the remaining CH bits. LC3 is gated with BUFFER DELAY (XFER INIT delay 100 ns) to produce C3.

C3 produces CLR X which clears the display X-Position Register (refer to drawing BS-D-338-0-6, sheet 1).

C3 and CHARM trigger 35 μs CR DELAY necessary for worst case (right edge to left edge) dot return. The termination of the delay produces CR DONE which, in turn, sets the CHAR DONE flip-flop to produce BYTE DONE.



#### 4.10 LF (LINE FEED) SIGNAL FLOW

LF is a SPECIAL character which moves the dot and further information to be displayed down one line on the display CRT.

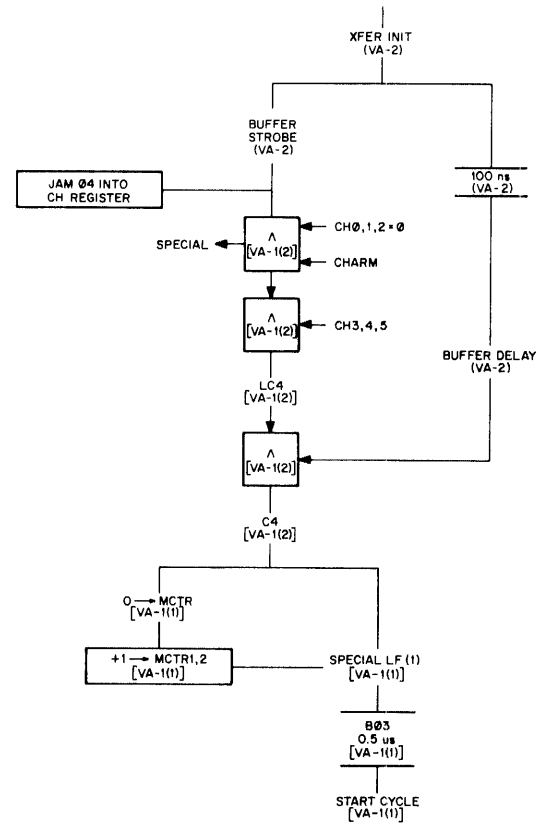
When LF (octal code 45) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC4 to be produced from the remaining CH bits. LC4 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C4.

C4 clears the MCTR, sets the SPECIAL LF flip-flop and triggers a 0.5  $\mu$ s delay.

By clearing the MCTR and then setting MCTR1 and MCTR2, the ROM address 0014 is specified.

Referring to Figure 4-2, ASCII Character Set, common character words can be seen at the specified address.

The termination of the 0.5  $\mu$ s delay produces START CYCLE. Operations continue as with common character generation with the exception that CHAR DONE (0) is true. ENABLE, necessary for the continuation of the timing chain, is now produced by C4 rather than by CHAR DONE (1).



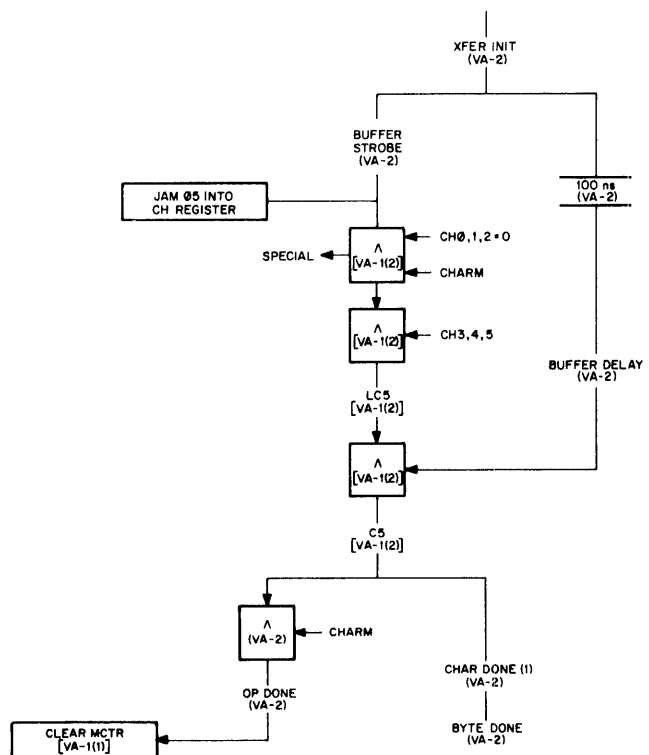
#### 4.11 ESC (ESCAPE) SIGNAL FLOW

ESC is a SPECIAL character which allows the display to leave character mode.

When ESC (octal code 46) is executed, logic operations similar to those of common character generation address the ROM and jam transfer the first character word into the CH REGISTER. CH0 and CH1 and CH2 will contain 0. This condition and CHARM will enable the binary to octal decoder, thereby permitting LC5 to be produced from the remaining CH bits. LC5 is gated with BUFFER DELAY (XFER INIT delayed 100 ns) to produce C5.

C5 and CHARM produce OP DONE to clear the MCTR. C5 also sets the CHAR DONE flip-flop to produce BYTE DONE.

OP DONE becomes OP DONE D in the display (refer to drawing BS-338-0-20) and is gated with LC5 to produce SET CYC 1.



CHAPTER 5  
MAINTENANCE

Preventive and corrective maintenance of the VA38 is simplified by the use of diagnostic program techniques. The following procedure can be used in both instances.

- a. Connect the VA38 - 338 cables according to the information provided in Figure 3-2 and Table 3-1 in Section 3 of this manual.
- b. Check for +5V at pin B02J.
- c. Set the reset break request delay to 500 ns. Set the INTENSIFY TIME delay M25 to 100 ns. These are all found in the 338.
- d. Load MAINDEC-08-D8MA. Run Section 00.
- e. Temporarily ground pin A25V (VA38). The graphic timing chain will be inhibited to allow the checking of single read only memory bytes.
- f. Check the following pulses: CODE AVAIL, START CYCLE, READ DELAY, XFER INIT, BUFFER STROBE, and BUFFER DELAY. Sync at pin B31M.
- g. Check memory inputs at the following pins: A31-H, M, F, E, P, D, N, T, R and S. The following pattern should be found.
 

0V	5V	5V	0V	0V	5V	5V	5V	5V	5V
	4			6					
- h. Check the START CYCLE pulse at pin A31J. Sync at pin B11F.
- i. Check for the pattern (46) described in Step g at CH0 through CH5. Sync at pin B12F.
- j. Check CH5 for proper decoding. NOTE: With SW0 = 0 and SW1 = 1. If the character generator is operating properly, the Y REGISTER and the X REGISTER of the 338 should contain 1000 and 1070, respectively. A visual check can be made via the indicator lights.
- k. Run Section 01 of MAINDEC-08-D8MA.
- l. Remove the temporary ground at pin A25V. Toggle 56g into the last six bits of the PDP-8 SWITCH REGISTER.
- m. Check for proper number of steps and direction decoding.
- n. Check all characters. Place emphasis on the SPECIAL characters 44 and 45, carriage return and line feed, respectively.
- o. Run Sections 10 and 11 of MAINDEC-08-D8MA.
- p. Rerun Section 10 of MAINDEC-08-D8MA. Determine the total time to generate one complete character set by measuring the time pin B31M remains continuously at ground. Divide this time by 68. The resulting time must not exceed 21.5  $\mu$ s.
- q. Rerun Section 01 of MAINDEC-08-D8MA. Measure the time between pulses at pin B26F. This is STEP TIME and must not exceed 1.1  $\mu$ s.



CHAPTER 6  
MAINTENANCE PARTS LIST

6.1 MODULES

Contained herein is information pertinent to replace-  
able items associated with the VA38 option.

Table 6-1 contains DEC module quantity, description  
and type information.

Table 6-1  
Module List

Quantity	Description	Type	Page
1	Diode Network	R001	7-2
3	Diode Network	R002	7-2
1	Inverter	R107	7-3
7	Expandable NAND/NOR Gate	R111	7-3
2	NAND/NOR Gate	R113	7-4
1	Input Bus	R123	7-4
6	Dual Flip-Flop	R202	7-5
1	Dual Delay Multivibrator	R302	7-5
1	Pulse Amplifier	R601	7-6
3	Pulse Amplifier	R602	7-6
2	Pulse Amplifier	R603	7-7
5	Inverter	B104	7-7
2	Inverter	B105	7-8
3	Inverter	B123	7-8
1	Inverter	B124	7-9
5	Delay (One Shot)	B301	7-9
1	Power Inverter	B681	7-10
1	Clamped Load	W005	7-10
1	Positive Level Converter	W512	7-11
2	Positive Level Converter	W603	7-11
1	Power Supply	W704	7-12
1	Quadruple Flip-Flop	B204	7-12

## 6.2 SPECIAL MODULE

### 6.2.1 Type 4698 Intensity Amplifier

The VA38 option contains a DEC Type 4698 Intensity Amplifier module which is a high speed replacement of the 4688 Intensity Amplifier used in 338 and 339 display systems. Use of the 4698 permits about 20% faster incremental plotting speed and individual adjustment of each of the eight intensity levels. The 4698 is required in 338/339 systems having a VA38/VA39 and is optional in other 338/339 systems.

The 4698 allows a decrease in the intensity time from 300 ns to 100 ns allowing a total incremental point to point decrease from 1.1  $\mu$ s to .9  $\mu$ s. This decrease allows about 20% more information to be displayed. The 4698 also features individual adjustment of the light output on each of the eight programmable intensity levels. An advantage of this feature for example would be to have intensity level 7 (brightest), very bright for highly responsive light pen operation, but a smooth gray scale from intensity 6 to intensity 0.

### 6.2.2 Circuit Description

Transistors T2, T3, T4 serve to convert the single rail inputs from the intensity register to double rail signals needed to drive the binary to octal converter. Transistor T1 is a simple inverter driving a "totem-pole" type output stage comprised of transistors T13 and T14. Transistor T13 is normally biased off. The leading edge of the input pulse turns T13 on and T14 off, causing a fast fall time at the output port, Pin 8. When the trailing edge is encountered, transistor T13 is turned off and T14 on. A faster rise time results than is possible with a passive load on T13. Rise and fall times are about 40 ns for a 40V pulse.

Transistors T5 through T12 serve as a binary to octal decoder, selecting one of eight resistors corresponding to each of the eight intensity levels. Transistor T15 forms a constant current source and, when used in conjunction with the selected resistor from the binary to octal converter, develops a unique voltage corresponding to one of the eight intensity levels. This voltage then references the diode D40 with the power gain of transistor T16. As the output pulse attempts to go more negative than this reference voltage, the diode D40 acts as a clamp and holds the output pulse to the reference value.

The network made up by D39 and R27 serves to DC restore the output pulse. This pulse is then coupled to the CRT cathode causing the spot to be intensified.

### 6.2.3 Adjustment Procedure

Load and start "Lots of Little Pictures" at address 107. Place the oscilloscope probe on the yellow wire terminal found on the display component plate. Adjust the intensity level pulse to approximately +20V. Adjust the intensity level setting on the 1705 CRT Bias module, display location Z02, to obtain a minimum intensity level (0). CRT light output should be minimum at this point. Readjust the gain potentiometer on the 4698 module for an even grey scale; minor adjustment should be required.

Figure 6-1 is a photograph of the 4698 Intensity Amplifier module and serves to illustrate the position of the gain control and the eight resistors responsible for the setting of the eight discrete intensity steps of the display. A circuit schematic of the module is shown in Figure 6-2.

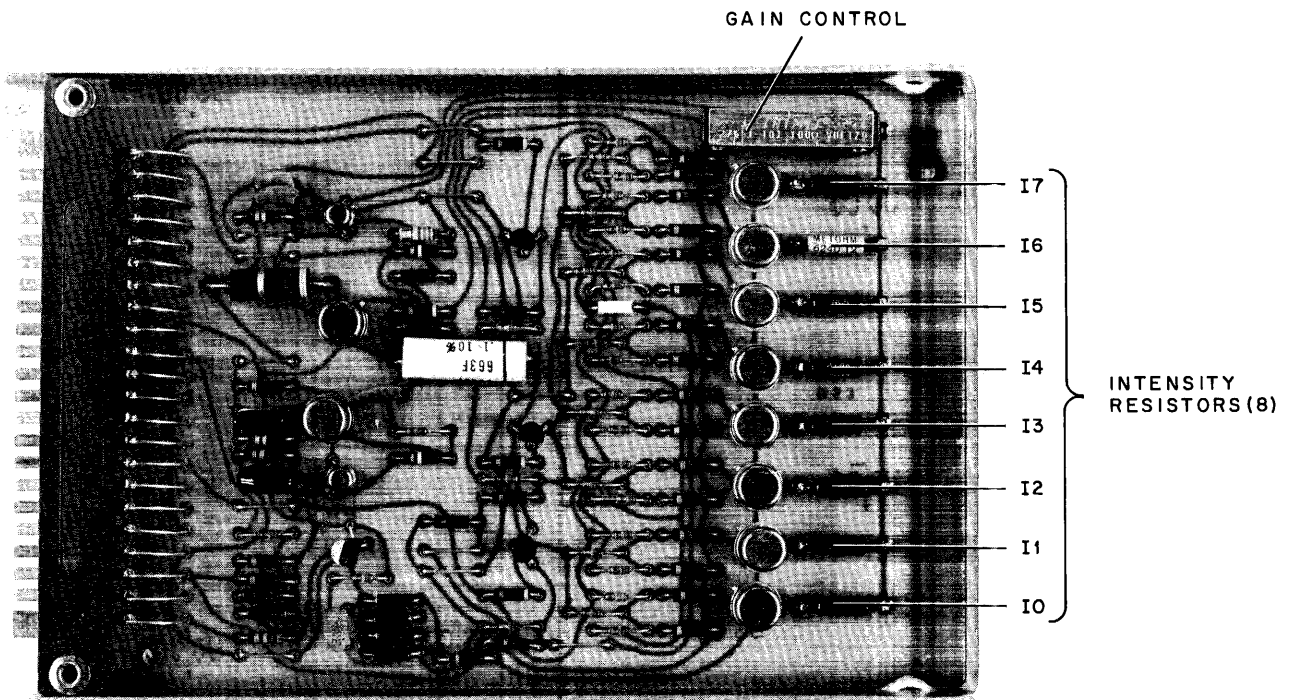
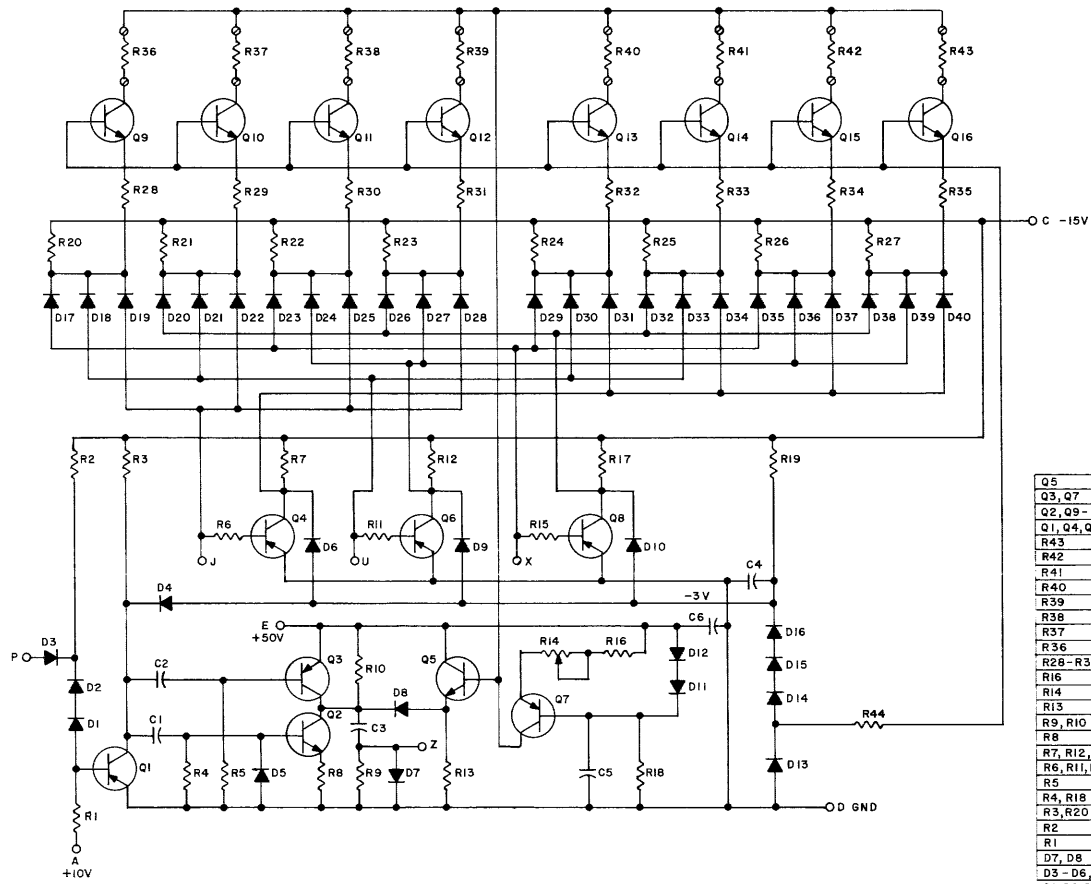


Figure 6-1 4698 Intensity Amplifier Module



6-4

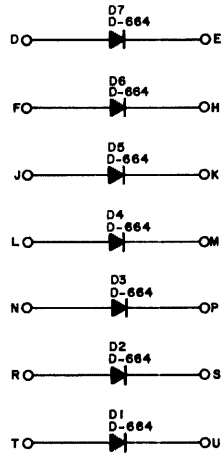


Q5	TRANSISTOR DEC3500-S	1503209
Q3, Q7	TRANSISTOR MM999-S	1501836
Q2, Q9-Q16	TRANSISTOR DEC2219-S	1501881
Q1, Q4, Q6, Q8	TRANSISTOR DEC3639-B	1502762
R43	RES. 4.02K 1/2W 1%	1309314-01
R42	RES. 4.22K 1/2W 1% 100MF	1309314-02
R41	RES. 4.42K 1/2W 1% 50MF	1309314-03
R40	RES. 4.64K 1/2W 1% 100MF	1309314-04
R39	RES. 4.99K 1/2W 1% 100MF	1309314-05
R38	RES. 5.36K 1/2W 1%	1309314-06
R37	RES. 5.76K 1/2W 1% 50MF	1309314-07
R36	RES. 6.49K 1/2W 1%	1309314-08
R28-R35	RES. 220 1/4W 10% CC	1300275
R16	RES. 47 1/4W 10% CC	1300204
R14	RES. 100 TRIMPOT	1305410
R13	RES. 4.7K 1W 10% CC	1301575
R9, R10	RES. 100K 1/4W 10% CC	1300534
R8	RES. 22 1/4W 10% CC	1300188
R7, R12, R17, R19	RES. 1.5K 1/4W 5% CC	1300391
R6, R11, R15	RES. 3K 1/4W 5% CC	1300432
R5	RES. 27K 1/4W 10% CC	1300508
R4, R18	RES. 10K 1/4W 10% CC	1300481
R3, R20-R27, R44	RES. 1K 1/4W 5% CC	1300365
R2	RES. 7.5K 1/4W 5% CC	1301422
R1	RES. 68K 1/4W 10% CC	1300526
D7, D8	DIODE D672	1105275
D3-D6, D9, D10, D17-D40	DIODE D664	1100114
D1, D2, D11-D16	DIODE D662	1100113
C6	CAP. .1MFD 100V	1002342
C3, C4, C5	CAP. .01MFD 100V 20% DISC	1001610
C2	CAP. 1000MMF 100V 5% MICA	1000042
C1	CAP. 47MMF 100V 5% D.M.	1000011
	PARTS LIST	A-PL-4698-0-0
REFERENCE DESIGNATION	DESCRIPTION	PART NO.
	PARTS LIST	

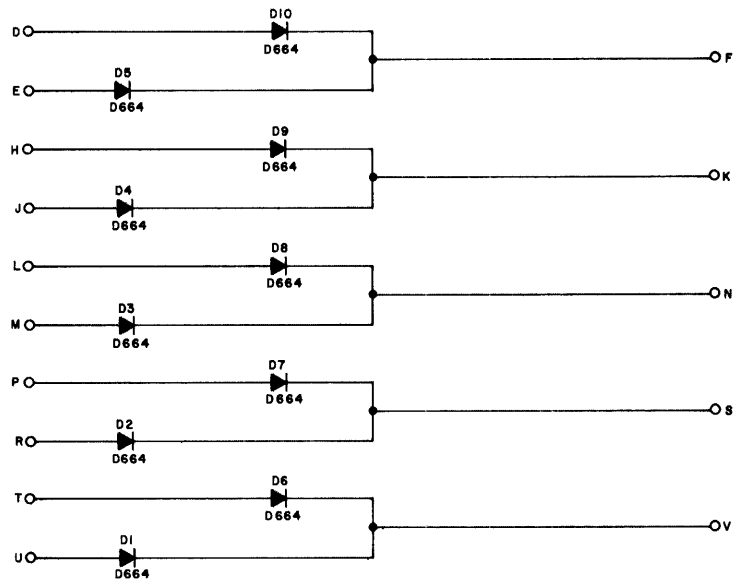
Figure 6-2 4698 Intensity Amplifier

CHAPTER 7  
ENGINEERING DRAWINGS

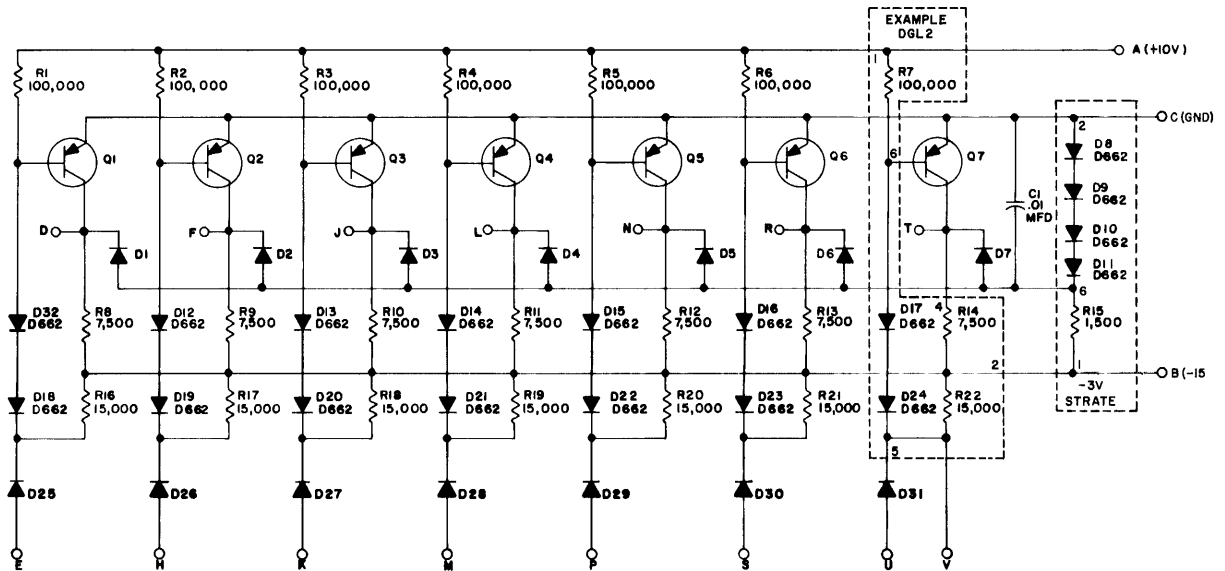
Drawing Number	Title	Revision	Page
D-UA-VA38-0-0	20 $\mu$ s Character Generator	-	7-13
A-PL-VA38-0-0	20 $\mu$ s Character Generator	-	7-15
C-AD-7005747-0-0	Wired Assembly	A	7-16
A-PL-7005747-0-0	Wired Assembly	A	7-17
D-BS-VA38-0-1	20 $\mu$ s Character Generator Decoding (2 Sheets)	B	7-19
D-BS-VA38-0-2	20 $\mu$ s Character Generator Timing	E	7-23
D-DI-VA38-0-4	Drawing Index List VA38	A	7-25
D-MU-VA38-0-6	Utilization Module List	B	7-27
A-PL-VA38-0-6	Utilization Module List (2 Sheets)	B	7-29
A-CP-VA38-0-7	External Components List	B	7-31



R001 Diode Network

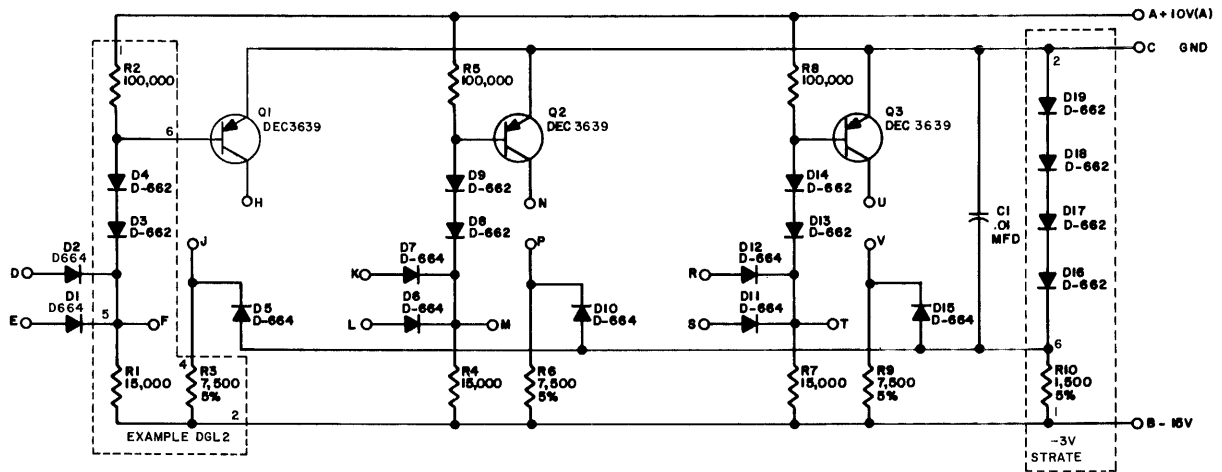


R002 Diode Cluster



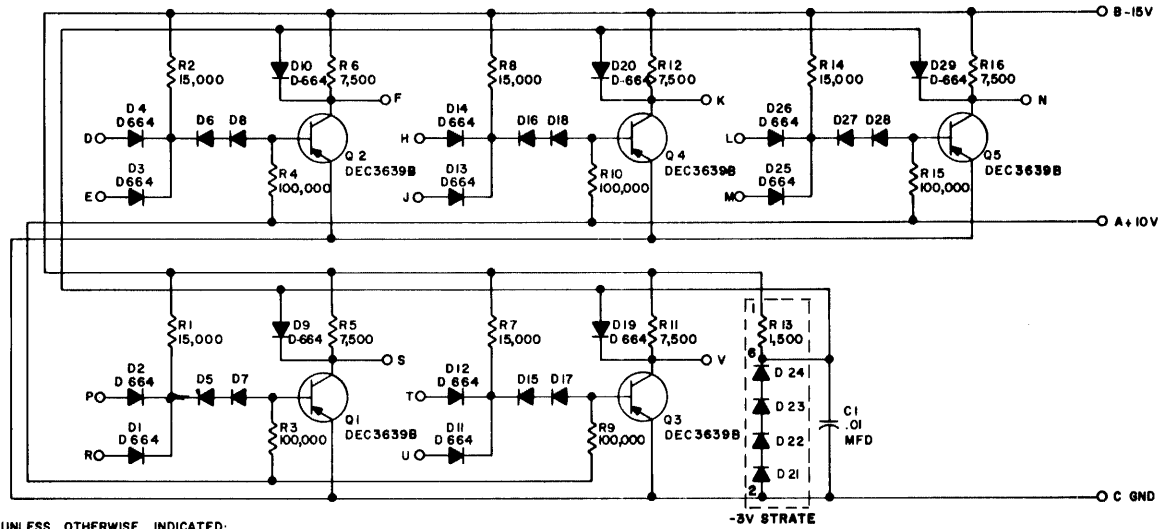
UNLESS OTHERWISE INDICATED;  
 RESISTORS ARE 1/4W, 5%  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639 B  
 PRINTED CIRCUIT REV. FOR  
 DGL BOARD IS SIA

R107 Inverter

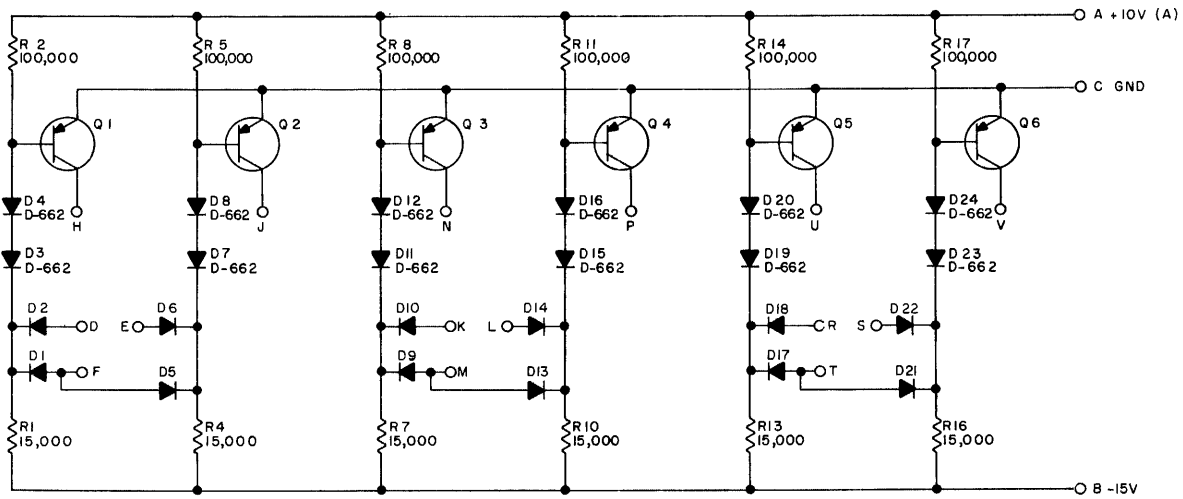


UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 PRINTED CIRCUIT REV. FOR  
 DGL BOARD IS SIB

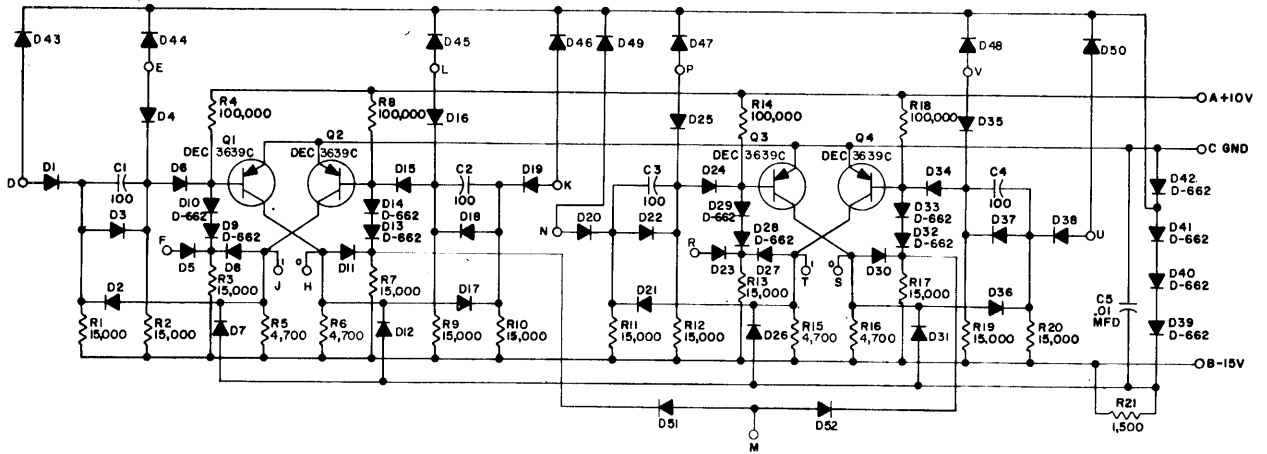
R111 Diode Gate



R113 Diode Gate

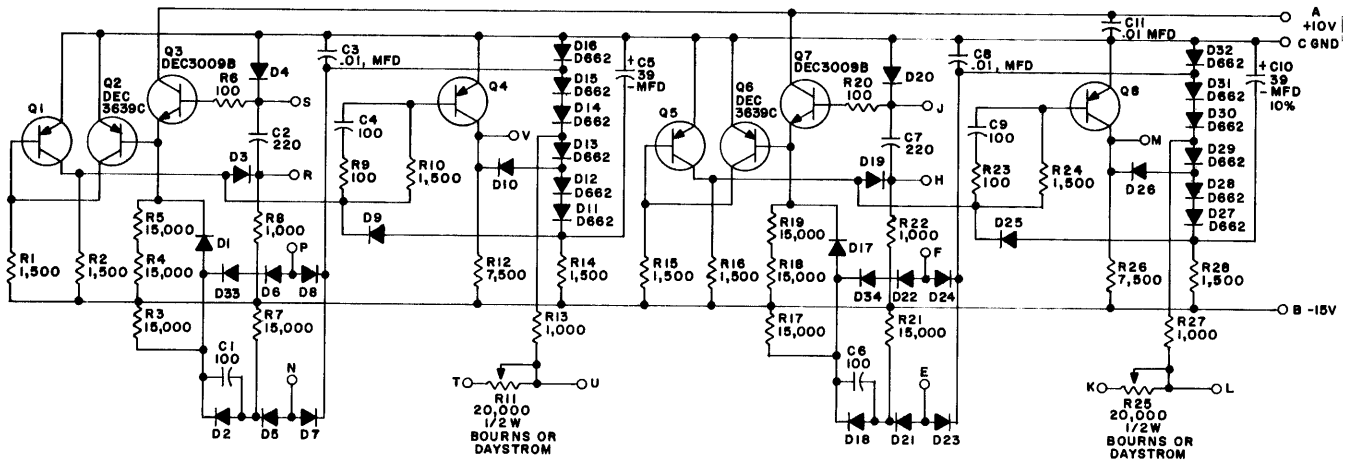


R123 Diode Gate



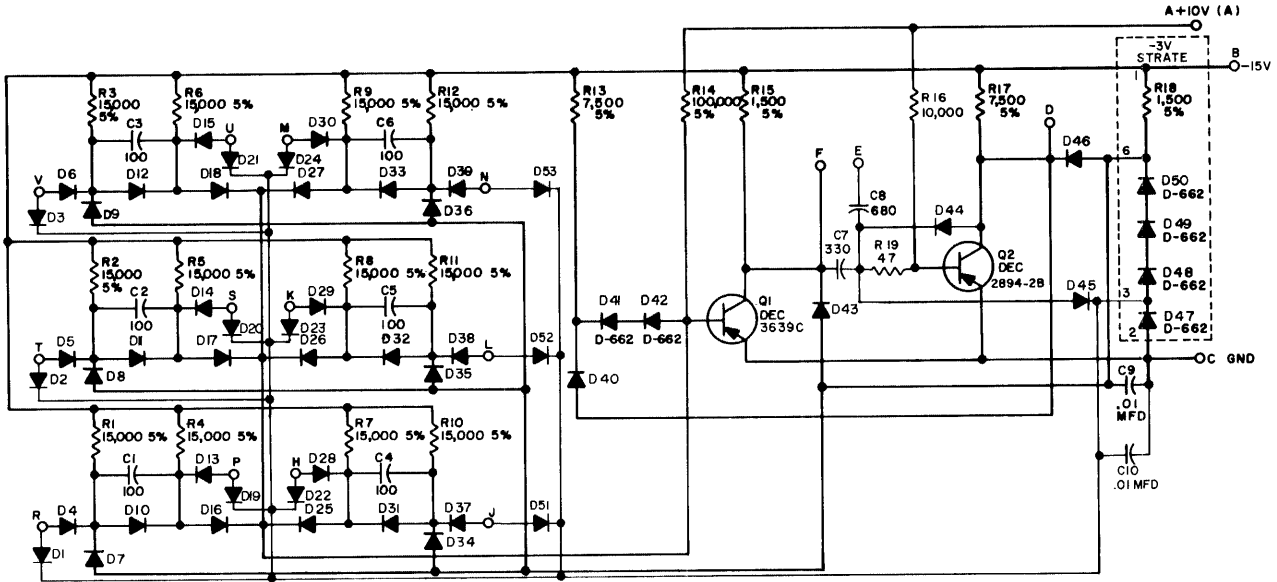
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664

R202 Dual Flip-Flop



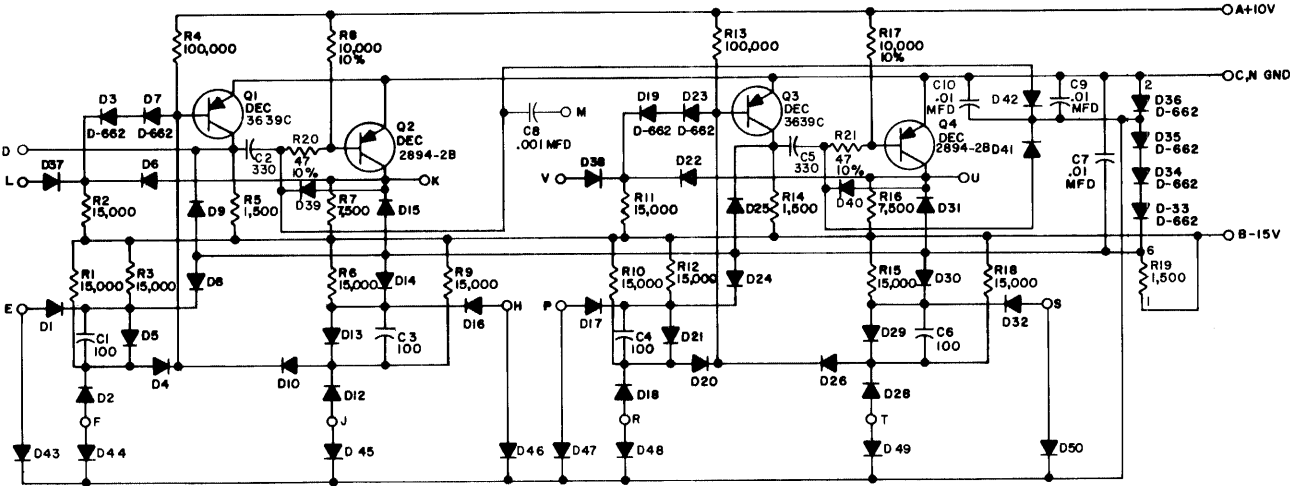
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D664  
 TRANSISTORS ARE DEC3639

R302 Dual Delay Multivibrator



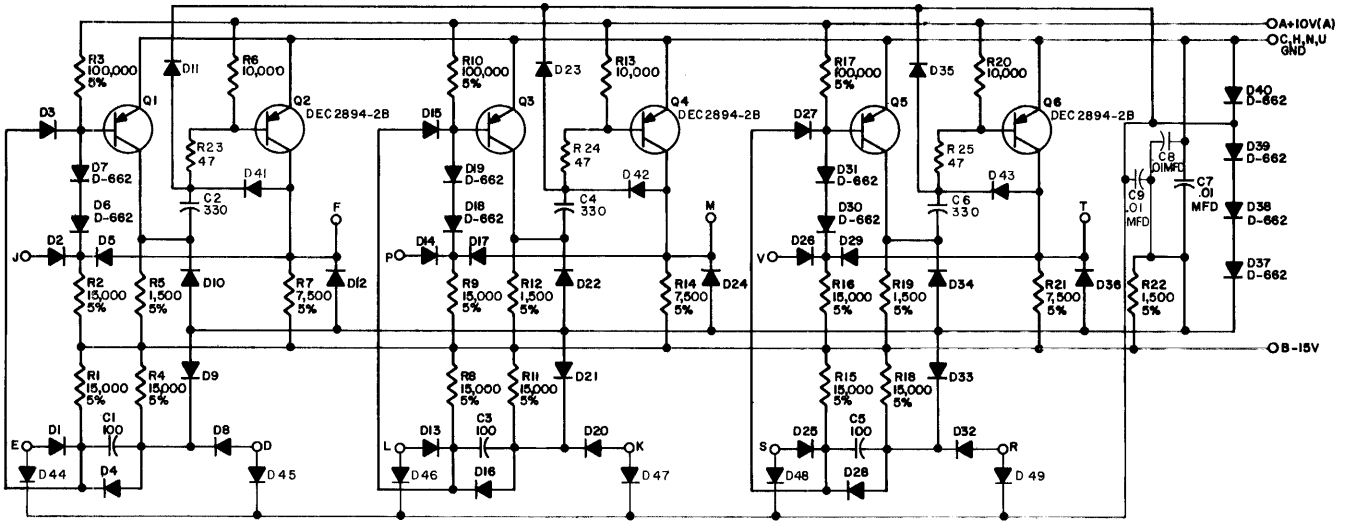
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 10%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664

R601 Pulse Amplifier



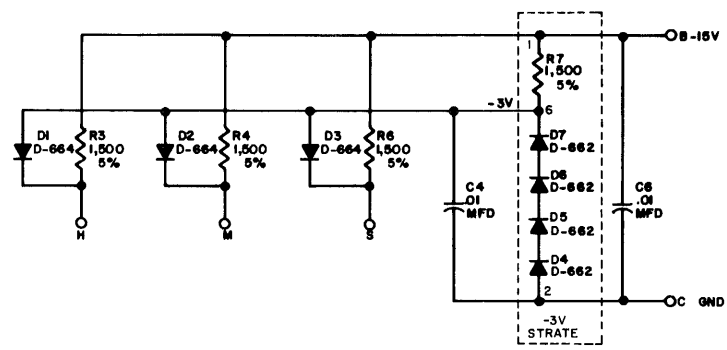
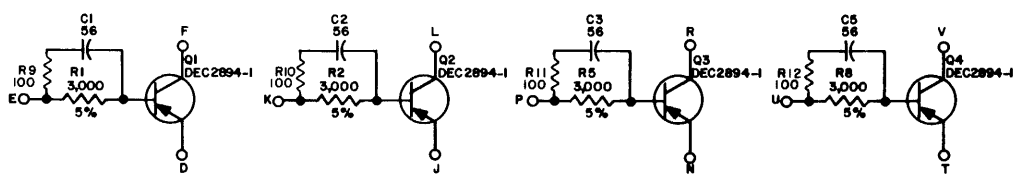
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664

R602 Pulse Amplifier



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W-10%  
 CAPACITORS ARE MMFD  
 DIODES ARE D-664  
 TRANSISTORS ARE DEC 3639-C

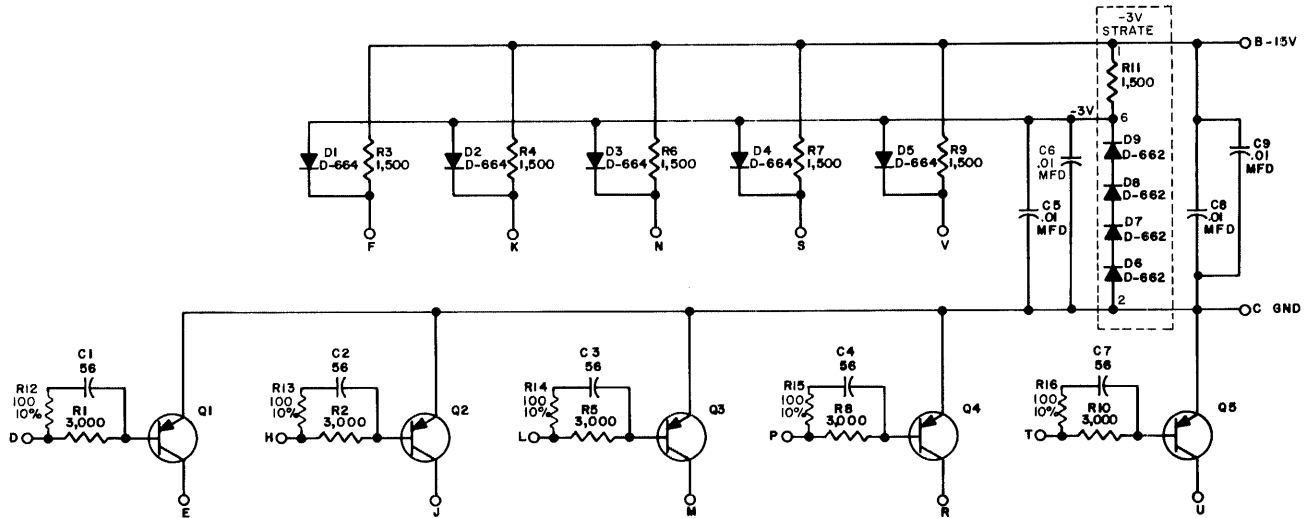
R603 Pulse Amplifier



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W-10%  
 CAPACITORS ARE MMFD

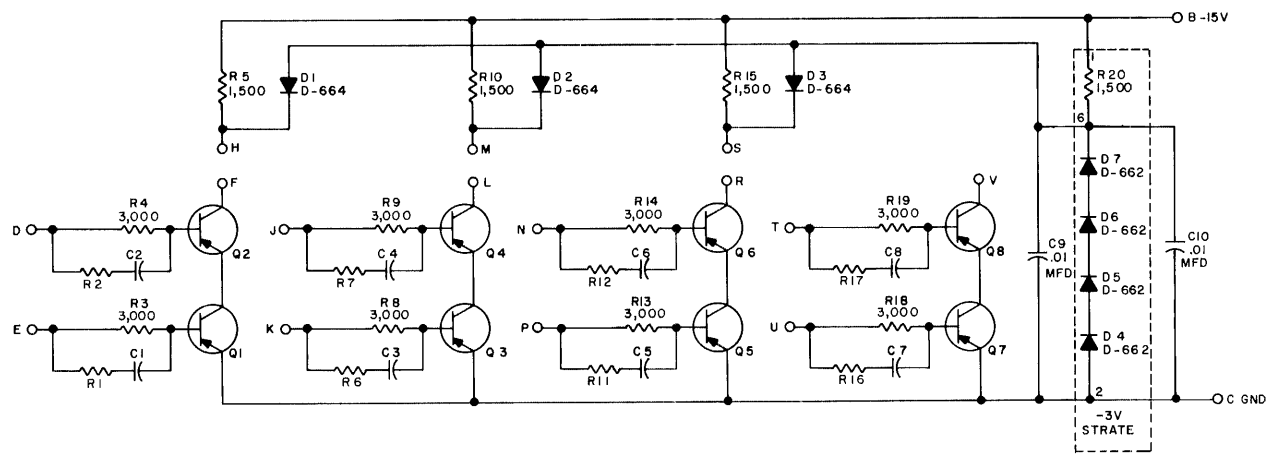
B104 Inverter





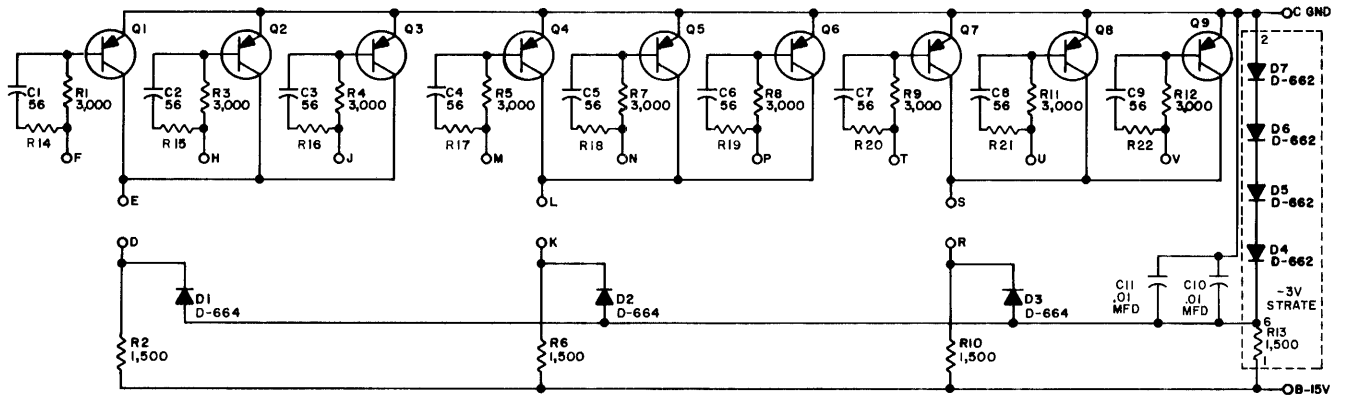
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 TRANSISTORS ARE DEC 2894-1B

B105 Inverter



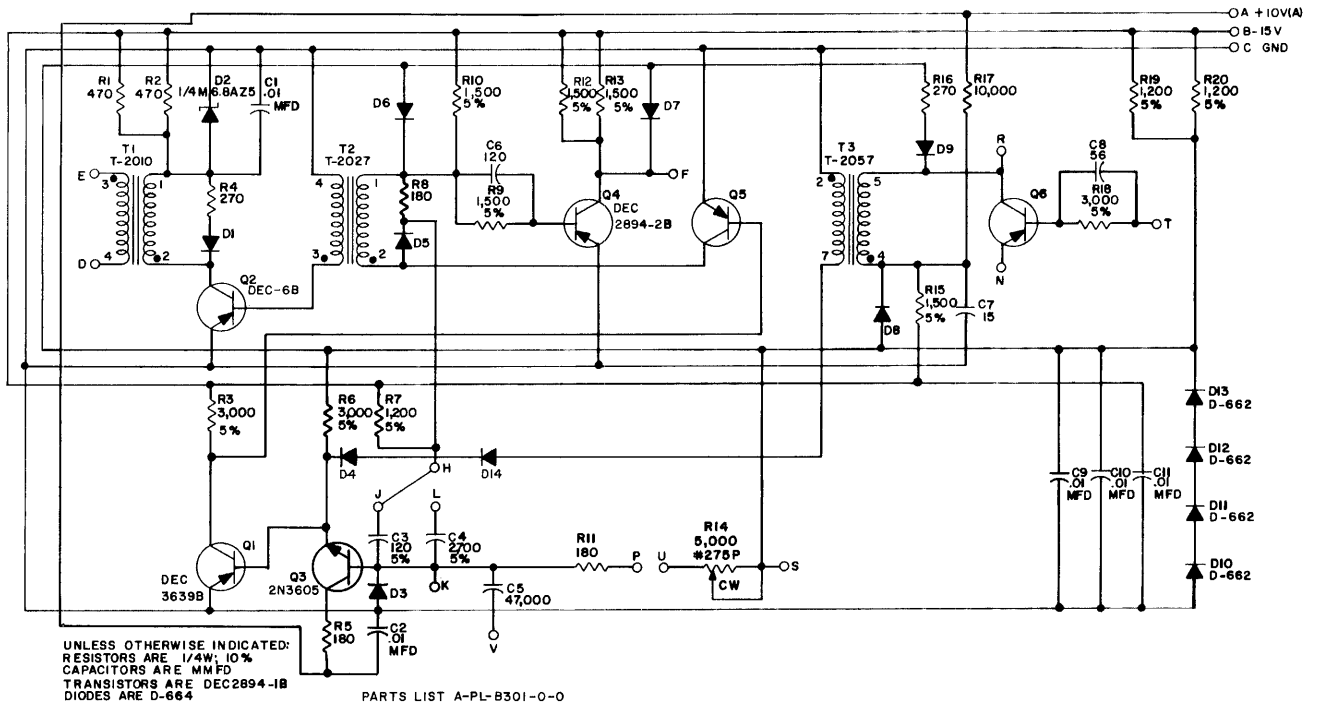
UNLESS OTHERWISE INDICATED:  
 CAPACITORS ARE 56 MMFD  
 RESISTORS ARE 1/4W, 5%  
 TRANSISTORS ARE DEC 2894-1  
 RESISTORS ARE 100, 1/4 W, 10%

B123 Inverter



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 TRANSISTORS ARE DEC 2894-1  
 RESISTORS ARE 100, 1/4 W, 10%

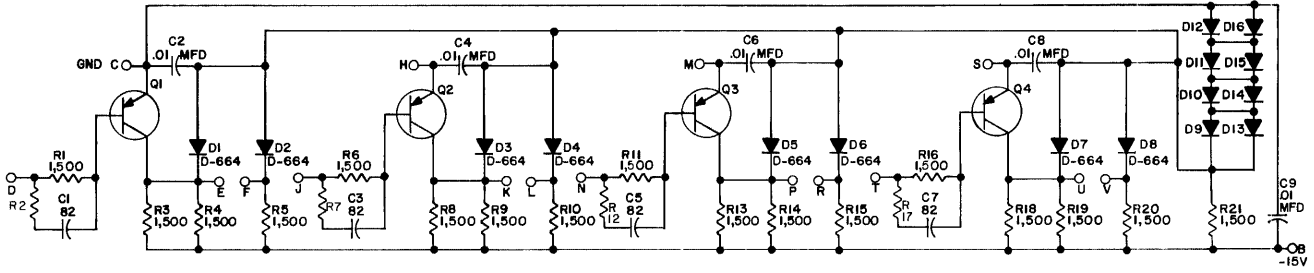
B124 Inverter



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 10%  
 CAPACITORS ARE MMFD  
 TRANSISTORS ARE DEC 2894-1B  
 DIODES ARE D-664

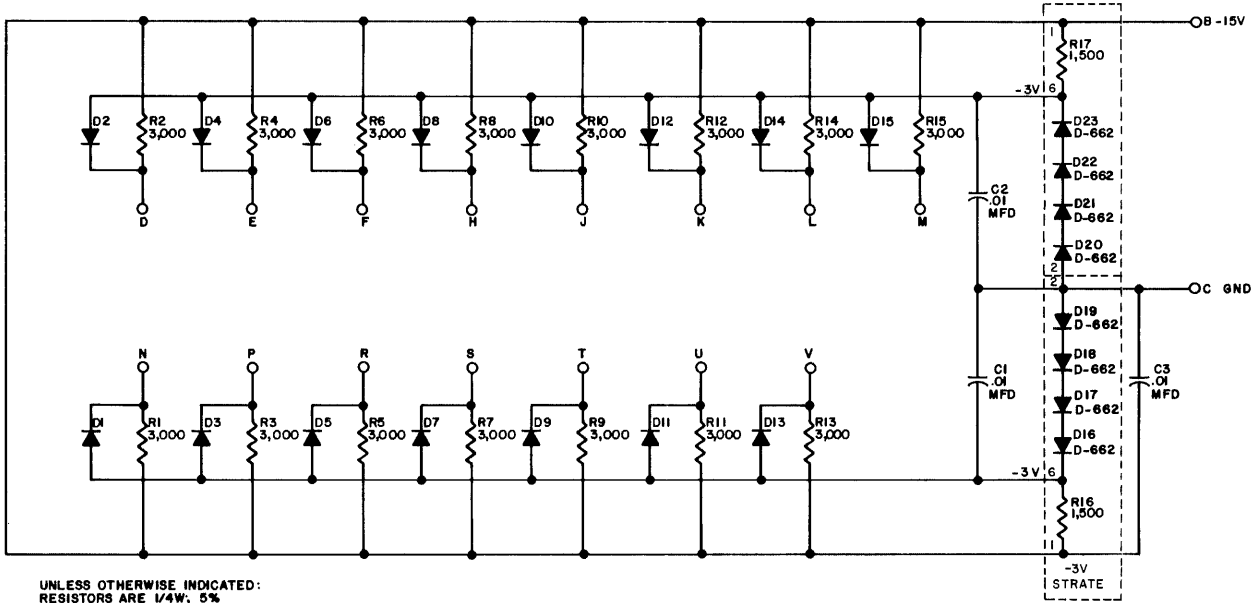
PARTS LIST A-PL-B301-0-0

B301 Delay (One Shot)



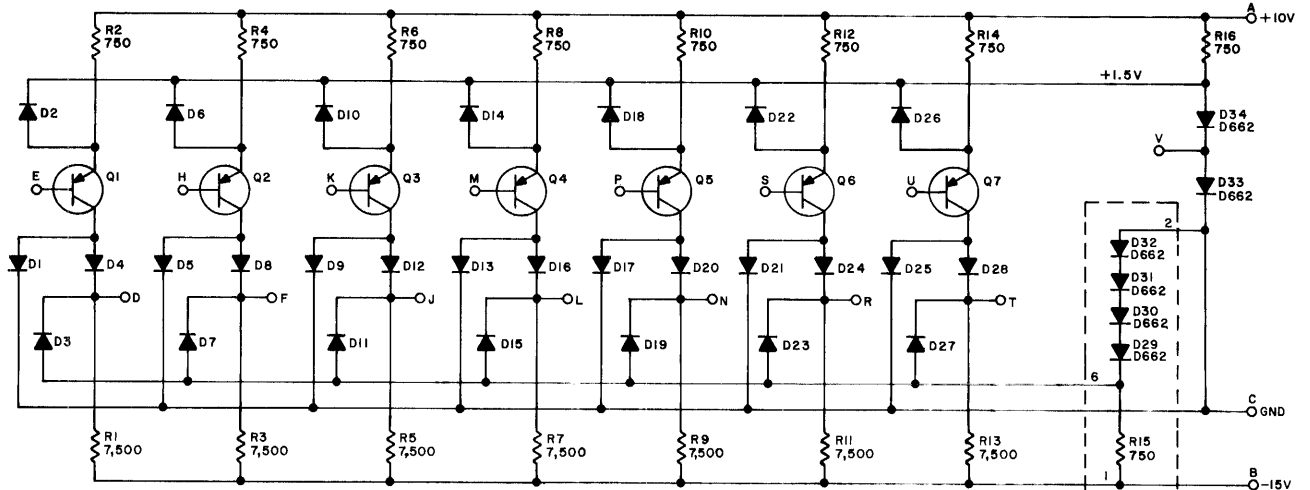
UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 CAPACITORS ARE MMFD  
 TRANSISTORS ARE DEC2894-2B  
 DIODES ARE D-662  
 RESISTORS ARE 100, 1/4W, 10%

B681 Power Inverter



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W, 5%  
 DIODES ARE D-664

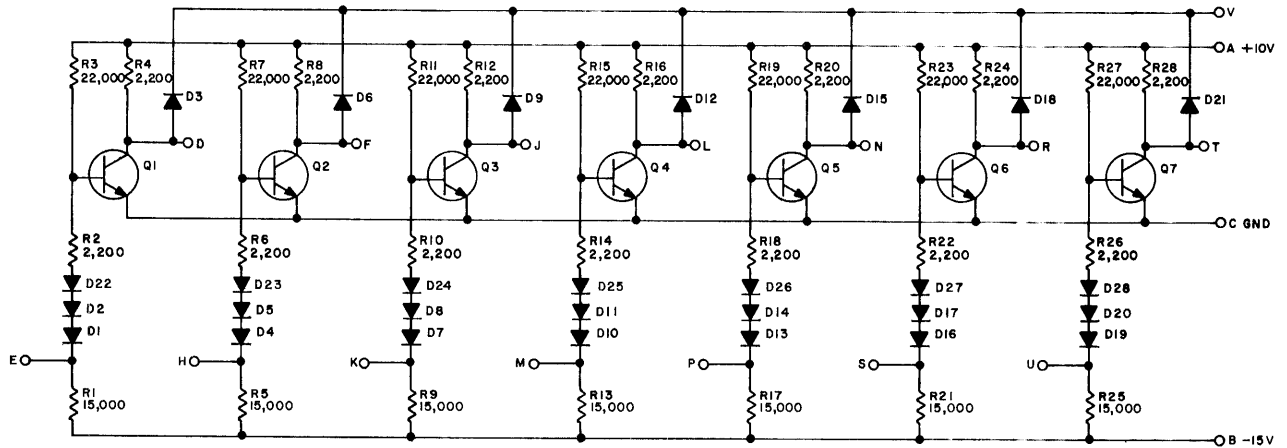
W005 Clamped Load



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W; 5%  
 DIODES ARE D664  
 TRANSISTORS ARE DEC3639B

(R15 IS 1,500 WHEN -3V  
 STRATE IS USED)

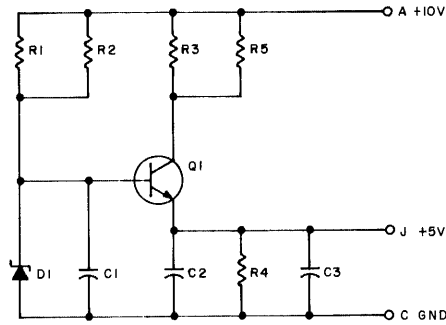
### W512 Positive Level Converter



UNLESS OTHERWISE INDICATED:  
 RESISTORS ARE 1/4W; 10%  
 DIODES ARE D664  
 TRANSISTORS ARE DEC3009B

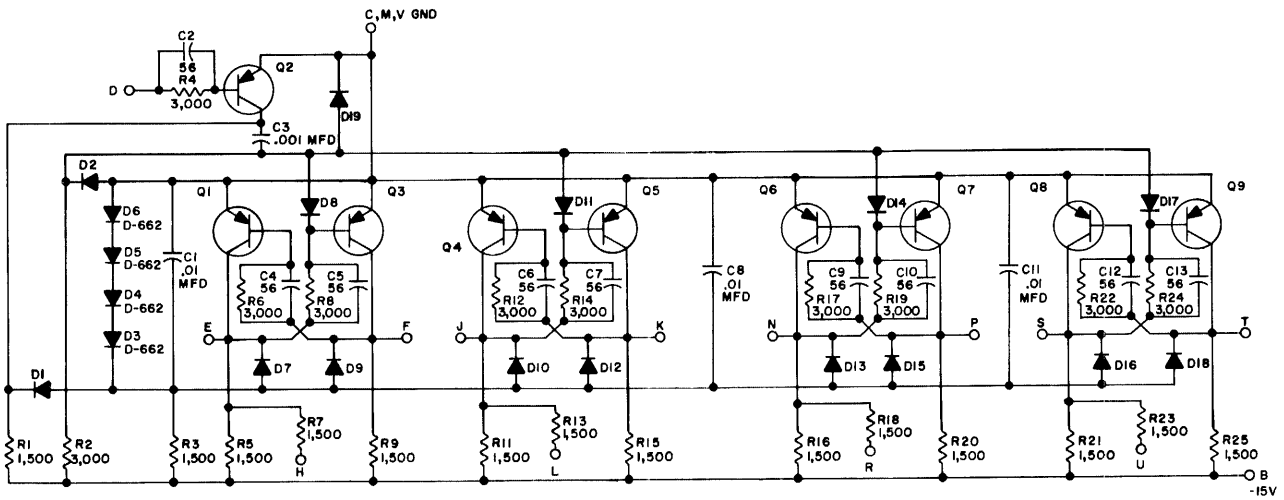
PARTS LIST A-PL-W603-0-0

### W603 Positive Level Amplifier



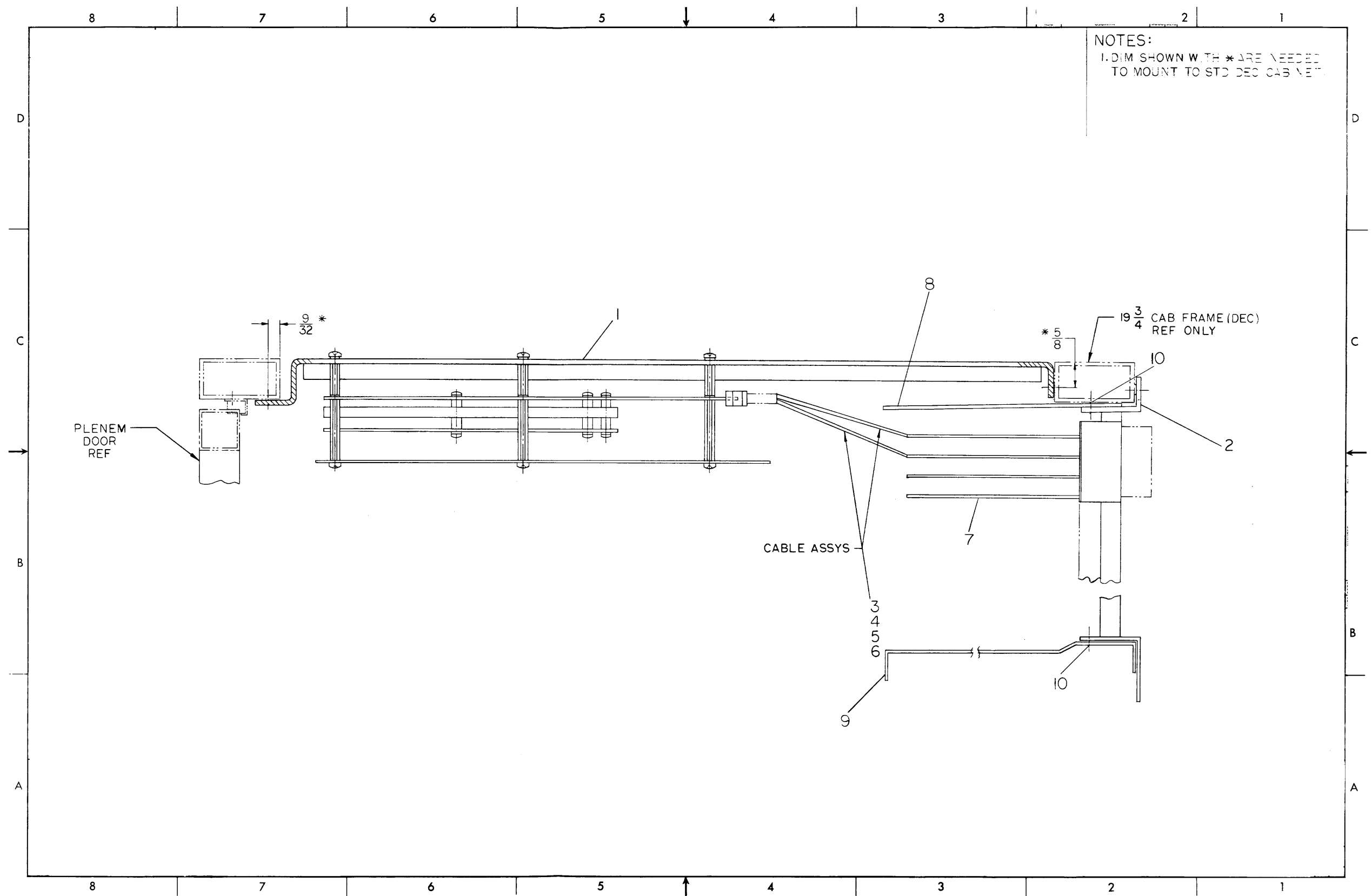
NOTE:  
Q1 IS MOUNTED ON A WAKEFIELD HEAT SINK 680-.75K

### W704 Power Supply



UNLESS OTHERWISE INDICATED:  
RESISTORS ARE 1/4W, 5%  
DIODES ARE D-664  
CAPACITORS ARE MMFD  
TRANSISTORS ARE DEC2894-1B

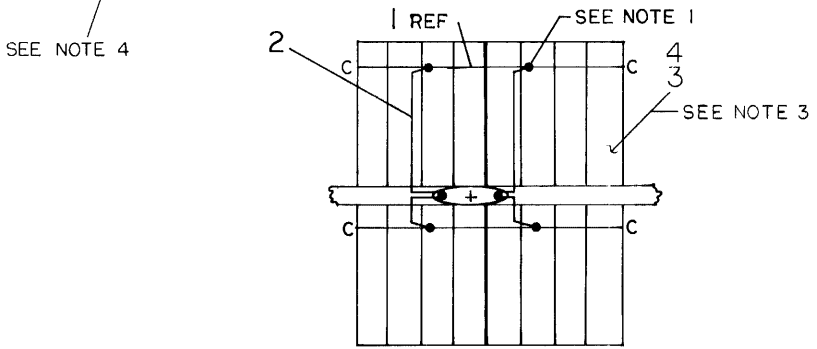
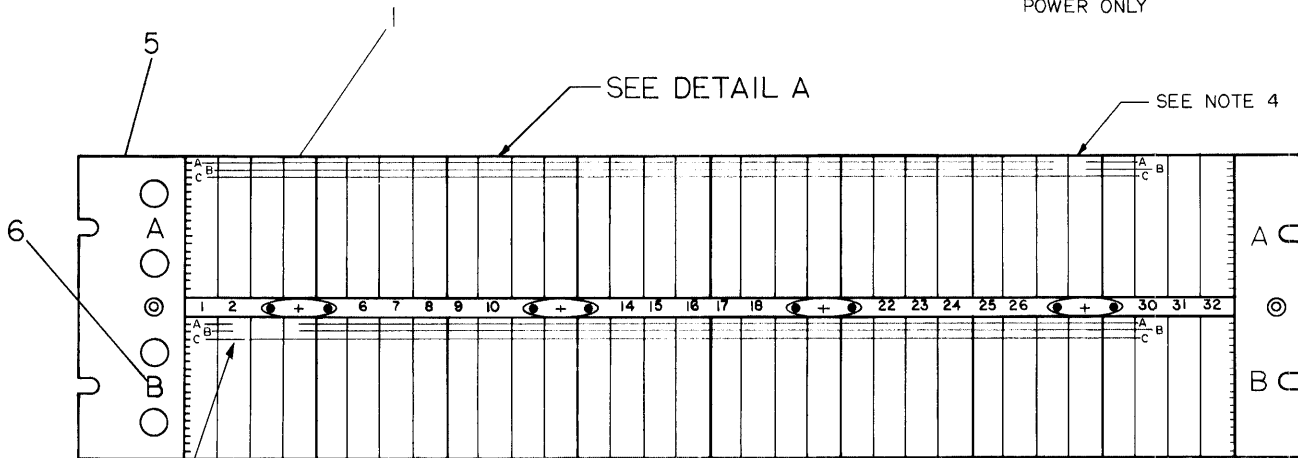
### B204 Quadruple Flip-Flop



<b>PARTS LIST</b>		<b>DIGITAL EQUIPMENT CORPORATION</b> MAYNARD, MASSACHUSETTS		
PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION ITEM — STOCK SIZE — CAT. NO. — MFG.	DEC. STOCK NO.
1	E-AD-7005783-0-0	1	MEMORY ASSY	7005783
2	C-AD-7005747-0-0	1	WIRED ASSY	7005747
3	C-IA-7405151-1-0	1	COMMAND CONNECTION	7405151-1
4	C-IA-7005814-0-0	1	CABLE ASSY W023-W023	7005814
5	C-IA-7005815-0-0	1	CABLE ASSY 80 PIN CINCH-W023	7005815
6	C-IA-7005816-0-0	1	CABLE ASSY W023-80 PIN CINCH	7005816
7	A-PL-VA38-0-6	REF	MODULE UTILIZATION LIST	
8	C-MD-5302486-0-0	1	RIGHT END PANEL	5302486
9	C-IA-5402526-0-0	1	MARGINAL CHK ASSY	5402526
10		8	POP RIVET AD43BS USMC	9006509

NOTES:

1. CONNECTIONS ON ITEMS \*1 & \*2 TO BE SOLDERED AND LOCATED AT MINIMUM PRACTICAL HEIGHT ABOVE BOARD.
2. ALL CONN BLOCKS TO BE GROUNDED TO GND LUGS AS SHOWN.
3. USE YELLOW WIRE (ITEM \*3) FOR MACHINE WRAPPED & BLUE WIRE (ITEM \*4) FOR HAND WRAPPED WIRING.
4. MODULE SLOTS B02, A28, A29, A30 WILL BE CONNECTED TO FIXED POWER ONLY



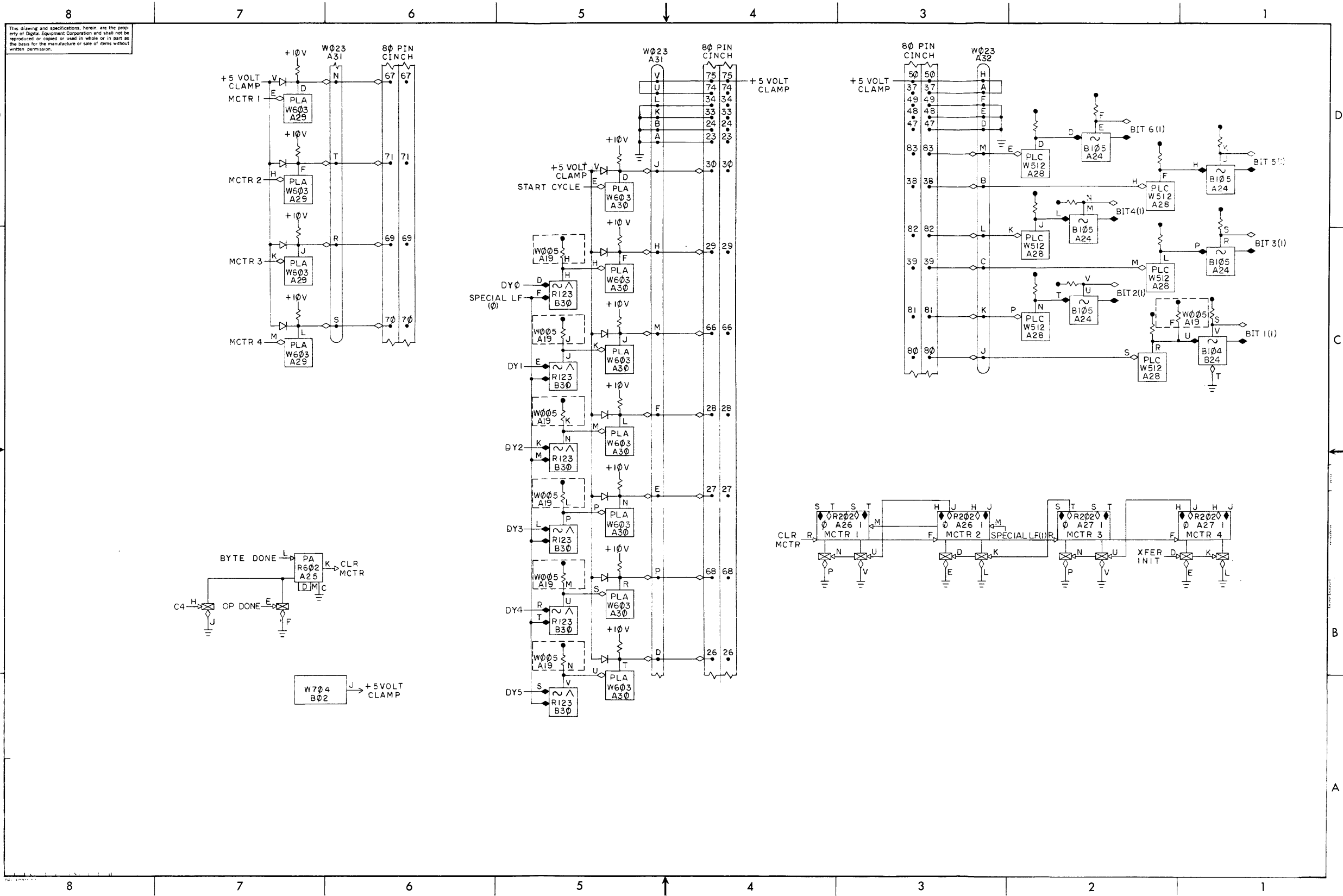
DETAIL A  
4 PLACES  
(SEE NOTE 2)

C-AD-7005747-0-0 Wired Assembly

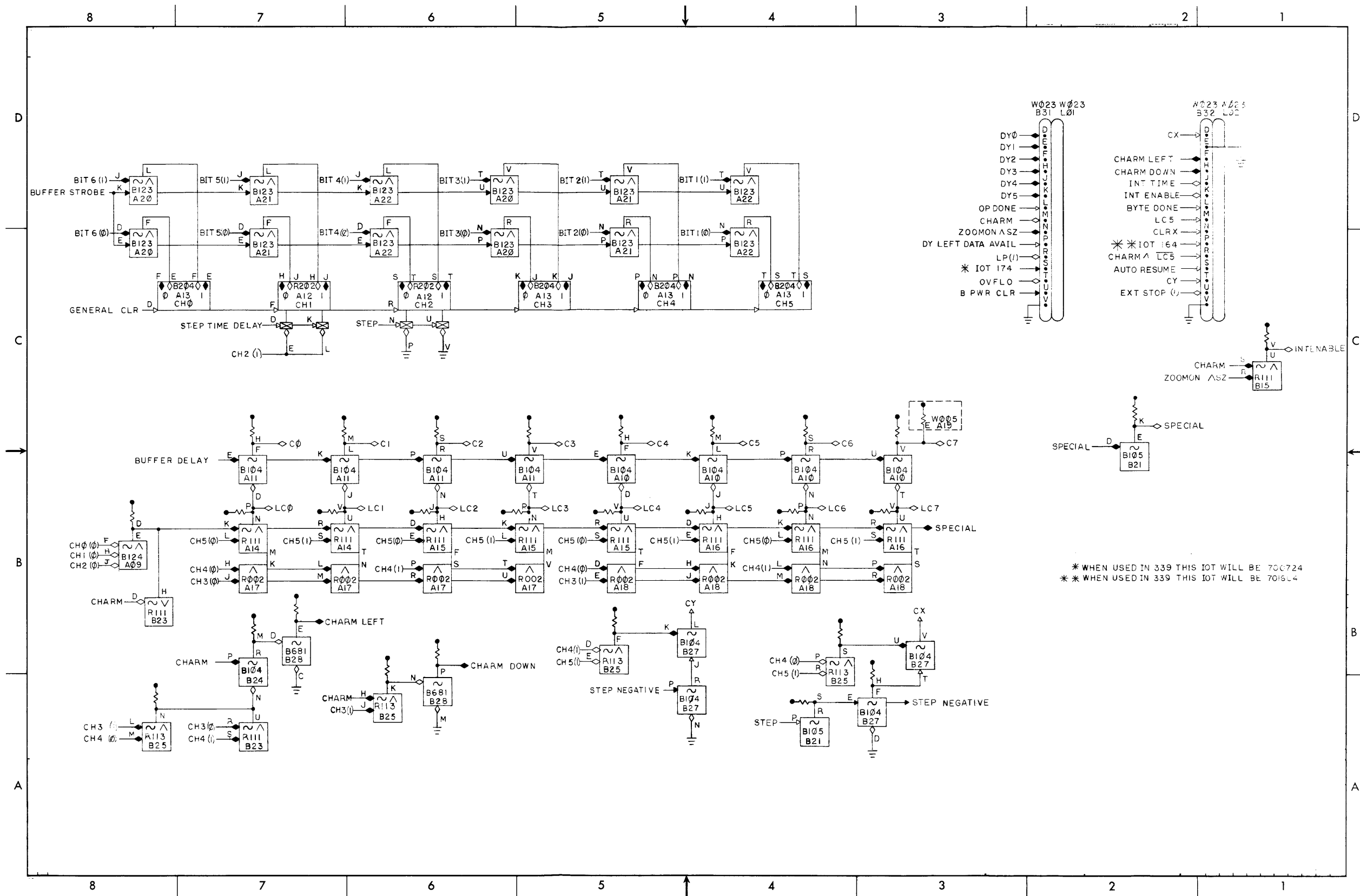


PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
1		A/R		VOLTAGE CHAIN	12-02188
2		A/R		#24 AWG SOLID WHITE WIRE	91-07470-1
3		A/R		#24 AWG SOLID YELLOW WIRE	91-07470-5
4		A/R		#24 AWG SOLID BLUE WIRE	91-07470-10
5	D-AD-1943-D-0	1		1943D MTG PANEL	1943D
6	A-DC-7406371-0-0	A/R		LOGIC FRAME DECAIS (CLEAR)	7406371
	SEE ML	REF		WIRE LIST (VA-38)	
	SEE ML	REF		EXTERNAL COMPONENTS LIST (VA-38)	

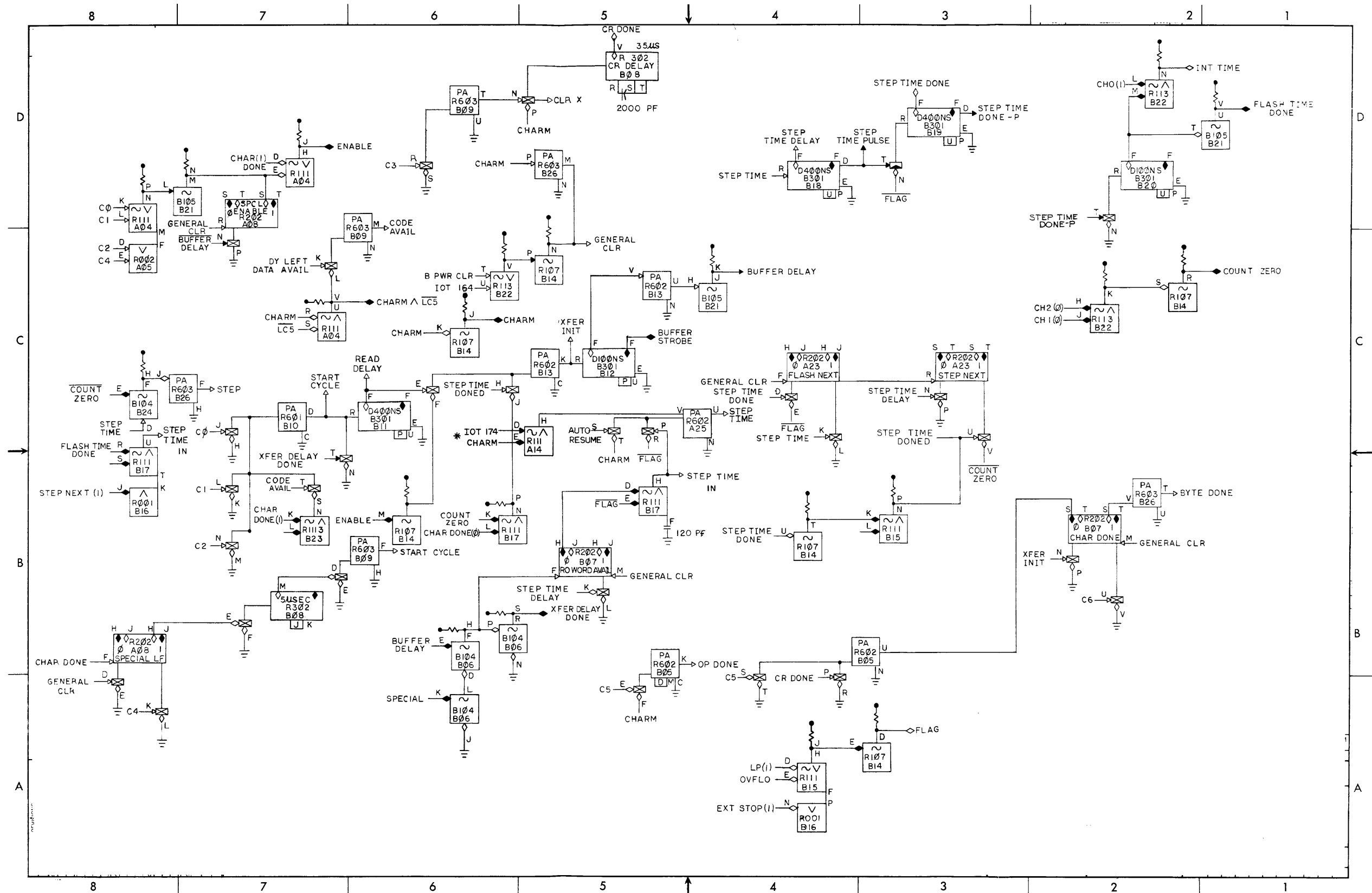
A-PL-7005747-0-0 Wired Assembly



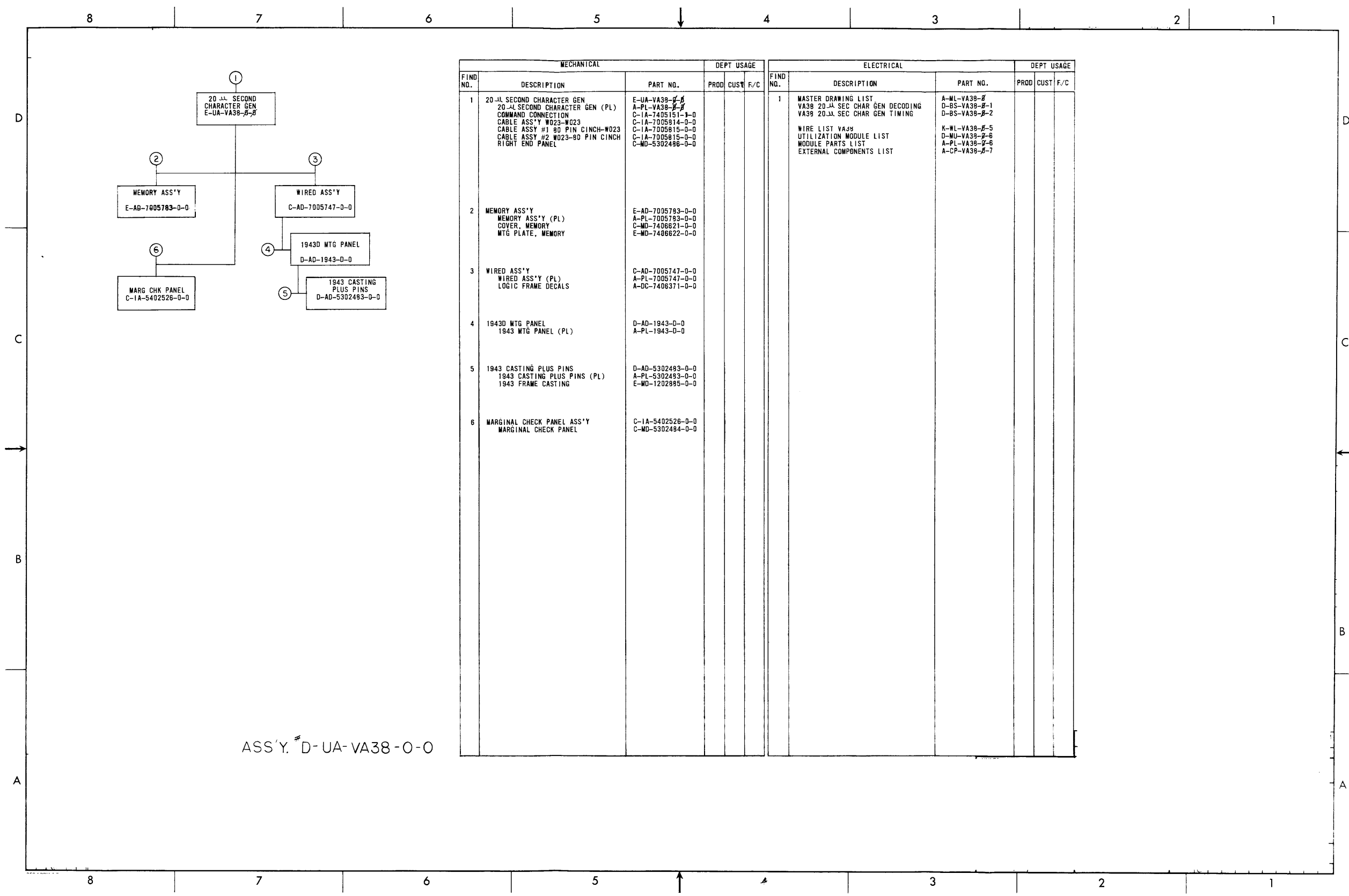
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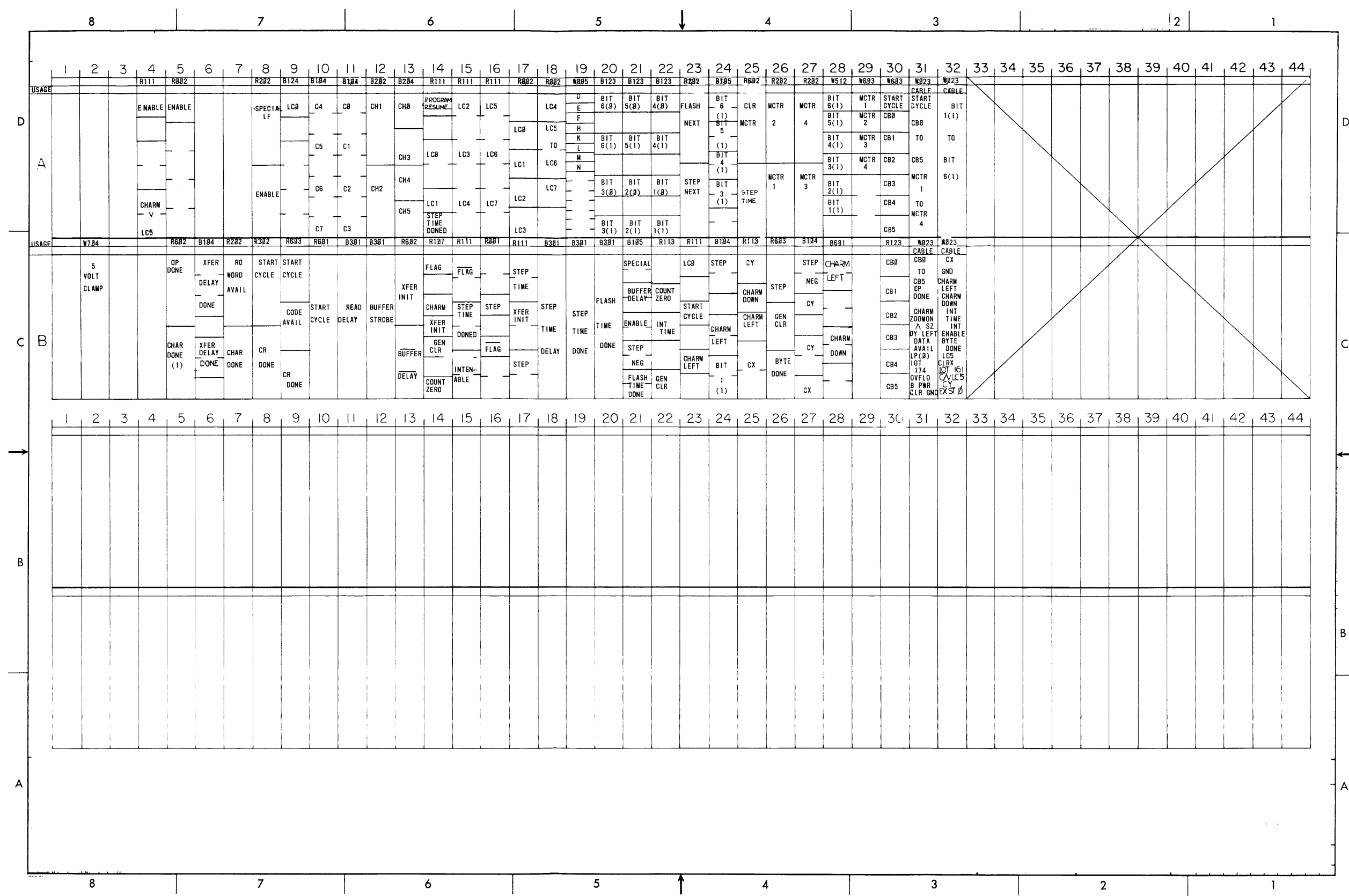
D-BS-VA38-0-1 20 μs Character Generator  
Decoding (Sheet 2)



D-BS-VA38-0-2 20 μs Character Generator Timing



ASS'Y. # D-UA-VA38-0-0



# PARTS LIST

# DIGITAL EQUIPMENT CORPORATION

MAYNARD, MASSACHUSETTS

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
		1	DIODE NETWORK		R001
		3	DIODE NETWORK		R002
		1	INVERTER		R107
		7	EXPANDABLE NAND/NOR GATE		R111
		2	NAND/NOR GATE		R113
		1	INPUT BUS		R123
		6	DUAL FLIP-FLOP		R202
		1	DUAL DELAY MULTIVIBRATOR		R302
		1	PULSE AMPLIFIER		R601
		3	PULSE AMPLIFIER		R602
		2	PULSE AMPLIFIER		R603
		5	INVERTER		B104
		2	INVERTER		B105
		3	INVERTER		E123
		1	INVERTER		B124
		5	DELAY (ONE SHOT)		B301

7-29

# PARTS LIST

## DIGITAL EQUIPMENT CORPORATION MAYNARD, MASSACHUSETTS

PART NO.	DRWG. NO.	NO. REQD.	DESCRIPTION		DEC. STOCK NO.
			ITEM	STOCK SIZE — CAT. NO. — MFG.	
		1	POWER INVERTER		ES11
		1	CLAMPED LOAD		W005
		1	POSITIVE LEVEL CONVERTER		W512
		2	POSITIVE LEVEL AMPLIFIER		W003
		1	POWER SUPPLY		W004
		1	FOUR FLIP FLOPS		R204

7-30





**Digital Equipment Corporation  
Maynard, Massachusetts**

