DEC 7000 AXP
VAX 7000
Technical Bulletin Number 3

Order Number EK–70TBA–T3. A01

This document accompanies the release of the KA7AB CPU module used in VAX 7000/10000 systems and the KN7AB CPU module used in DEC 7000/10000 systems.

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Preface

Intended Audience

This document is written for system managers and service engineers.

Document Purpose

This technical bulletin provides information to update the DEC 7000/10000 and VAX 7000/10000 documentation set. Since the original documentation set was published, we have issued two other Technical Bulletins, which are a part of the documentation set:

- *DEC 7000/10000 AXP Technical Bulletin Number 1*—EK–70TBA–T1
- *DEC 7000/10000 AXP Technical Bulletin Number 2*—EK–70TBA–T2

This document accompanies the release of two new modules for this platform. They are:

- KA7AB CPU module for VAX 7000/10000 systems
- KN7AB CPU module for DEC 7000/10000 systems

The following options are also described in this document:

- KFMSB adapter module—Supports DSSI buses on DEC 7000/10000 systems
- MS7AA-FA memory module—A 2-gigabyte memory module; supported on both VAX and DEC 7000/10000 systems.

Chapter 3 also provides the power requirements for newly supported options, used to determine when a second power regulator is needed.

If you have an Internet account, you may mail us your comments on VAX 7000/DEC 7000 hardware documentation. Please mail your comments, suggestions, and corrections to **msbdoc@lando.enet.dec.com.** *We will reply to all comments. Digital values your input.*

Section 1

Installation

The KA7AB and KN7AB processor modules can be used to upgrade VAX 7000/10000 and DEC 7000/10000 systems. The KA7AB module is used to upgrade VAX systems with KA7AA modules, and the KN7AB module is used to upgrade DEC systems with KN7AA modules.

Sections include:

- Changes
- System Upgrades

1.1 Changes

Alpha AXP systems are supported by OpenVMS AXP Version 6.1 and DEC OSF/1 Version 3.0. VAX systems are supported by OpenVMS VAX Version 6.1.

DEC Systems

The DECchip 21064A CPU chip on the KN7AB module provides improved performance over the DECchip 21064 chip. The chip speed is 275 MHz. Other features of the CPU chip, which differ from DECchip 21064, are the following:

- Instruction cache increased from 8 Kbytes to 16 Kbytes
- Data cache increased from 8 Kbytes to 16 Kbytes
- Parity protected internal caches
- Improved branch prediction logic
- Improved floating-point divide pipeline
- Some bit changes in internal processor registers

With the release of the KFMSB module, DEC systems now support DSSI subsystems.

VAX Systems

The NV5 CPU chip on the KA7AB module provides improved performance over the NVAX and NVAX+ chips. The CPU chip is implemented in CMOS-5 technology. The NV5 chip speed is 137.5 MHz compared with 91 MHz for the NVAX+ chip.

One internal processor register has changed: the BIU Control Register.

Both DEC and VAX systems now support the 2-Gbyte memory module.

Console Revision Requirements

KA7AB —V1.0 console release is required initially, until Version 3.5 is available, which provides support for both KA7AA and KA7AB modules.

KN7AB —V3.3 console release or later

KFMSB —V3.2 or later for DEC 7000 systems with KN7AA modules
V3.3 or later for DEC 7000 systems with KN7AB modules

MS7AA-FA —V3.2 or later for DEC 7000 systems with KN7AA modules
V3.3 or later for DEC 7000 systems with KN7AB modules
V3.2 or later for VAX 7000 systems with KA7AA modules
V1.0 or later for VAX 7000 systems with KA7AB modules

Correction to LFU Booting on DEC 7000

The Loadable Firmware Update (LFU) Utility is on the Alpha AXP Systems Firmware Update CD-ROM. To boot LFU from the InfoServer, enter the following command at the console prompt, supplying the version number for *nn*:

```
P00>>> boot exa0 -file AXP7000_Vnn
```

LFU starts, displays a summary of its commands, and issues its prompt (Function?).

1.2 System Upgrades

Upgrades can be of various types. Modules must be returned when the upgrade replaces the current CPU modules.

Upgrades can be of the following types:

- Upgrading from KA7AA modules to KA7AB modules
- Adding a KA7AB to an existing VAX system with KA7AB modules
- Upgrading from KN7AA modules to KN7AB modules
- Adding a KN7AB to an existing DEC system with KN7AB modules
- Upgrading from a VAX 7000 or 10000 system to a DEC 7000 or 10000 system.

Complete installation instructions are packaged with each CPU module.

NOTE: The numbering scheme for the OpenVMS AXP operating system has changed to match the OpenVMS VAX numbering scheme. The revision level required to support these CPU modules is Version 6.1 for both VAX and DEC systems.

Section 2

User Information

Changes to console commands:

- Set System_Variant

Changes to registers:

- KA7AB BIU Control Register
- KN7AB Cache Status Register
- KN7AB Abox Control Register
- KN7AB BIU Control Register

2.1 Console Commands

2.1.1 Set System_Variant

The default value for the system_variant environment variable is 0. After issuing a build EEPROM command on a DEC or VAX 10000 system, you must set the system_variant environment variable to a value of 1.

Example 2-1 Set System_Variant Command

```
P00>>> set system_variant 1    # Set system variant
                               # to 1 for DEC 10000.
P00>>>
```

The **set system_variant** command syntax is:

set[t] system_variant<value>

where **value** is one of the following:

- **0** for DEC 7000 and VAX 7000 systems (default)
- **1** for DEC 10000 and VAX 10000 systems

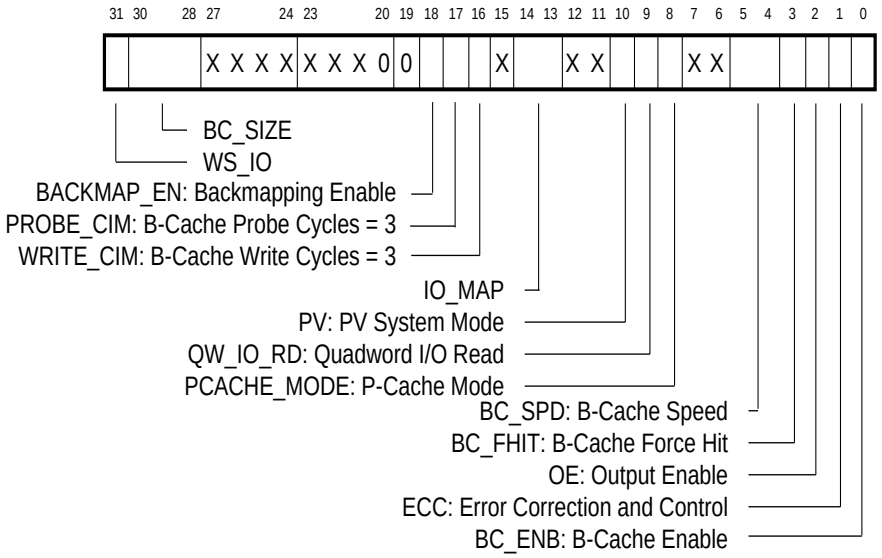
2.2 Registers

The following register information updates that given in the KA7AA and KN7AA CPU Technical Manuals. The registers described are on-chip registers.

KA7AB BIU Control Register (BIU_CTL)

Address 00A0
Access R/W

The BIU_CTL register controls certain operations and parameters related to the P-cache, B-cache, and I/O mapping. This register reads the complement of its contents.



NOTE: X bits read values from DIAG_CTL.
This register reads inverted.

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Table 2-1 KA7AB BIU_CTL Register Bit Definitions, Revised

Name	Bit(s)	Type	Function
BACKMAP_EN	<18>	R/W, 0	**Backmap Enable.** Controls whether internal IRead aborts, which have been backmapped, generate invalidates to the P-cache. The console program sets this bit to 1.
PROBE_CIM	<17>	R/W, 0	**Probe Cache Cycle Injection Mode.** Controls the number of CPU cycles for all B-cache probes when set. The console program sets this bit to 1, which allows all B-cache probe cycles to increase from 2 to 3 CPU cycles.
WRITE_CIM	<16>	R/W, 0	**Write Cache Cycle Injection Mode.** Controls the number of CPU cycles for all B-cache writes when set. The console program sets this bit to 1, which increases the assertion duration on the dataWE_h<3:0> and tagCtWE_h pins from 2 to 3 CPU cycles.

KN7AB Cache Status Register (C_STAT)

Address Abox 12
Access R

This register was named D-Cache Status Register in the DECchip 21064 (EV4 chip).

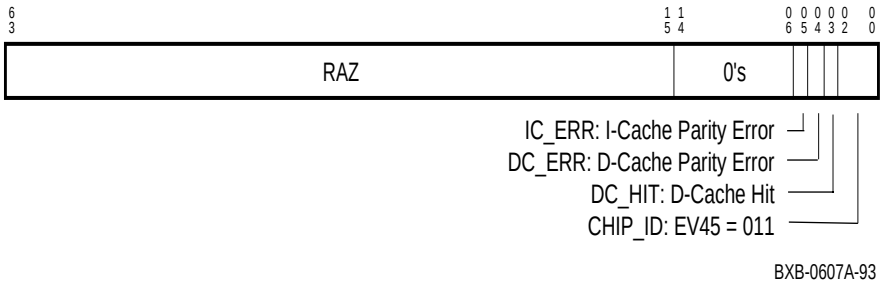


Table 2-2 KN7AB C_STAT IPR Bit Definitions, Revised

Name	Bit(s)	Type	Function
IC_ERR	<5>	R	**Instruction Cache Parity Error**. Set by I-cache parity error. Cleared by read of this register.
DC_ERR	<4>	R	**Data Cache Parity Error.** Set by D-cache parity error. Cleared by read of this register.
CHIP_ID	<2:0>	R	**Chip Identification.** This field has a value of 011 (bin).

KN7AB Abox Control Register (ABOX_CTL)

Index Abox 14
Access W

The ABOX_CTL IPR controls the Abox functions. PALcode writes to this register at initialization and keeps an image of the register which appears in error log entries and is readable by the user. The console initializes the D-cache to 16 Kbytes.

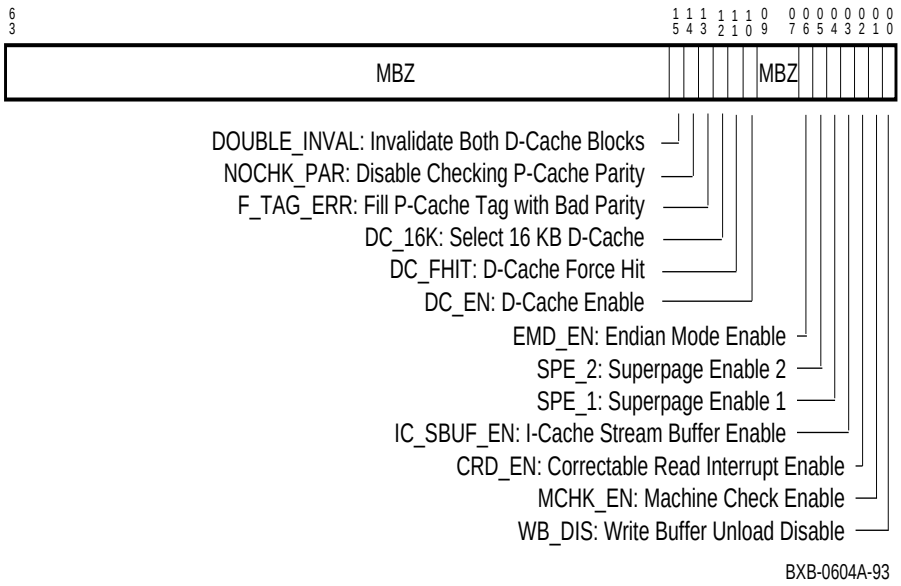


Table 2-3 KN7AB ABOX_CTL IPR Bit Definitions, Revised

Name	Bit(s)	Type	Function
DOUBLE_INVAL	<15>	W, 0	**Invalidate Both D-Cache Blocks.** When set, dInvReq_h<0> assertions invalidate both D-cache blocks addressed by iAdr_h<12:5>. Cleared by reset.
NOCHK_PAR	<14>	W, 0	**Disable Checking P-Cache Parity.** Set to disable checking of primary cache parity. Cleared by reset.
F_TAG_ERR	<13>	W, 0	**Fill P-Cache Tag with Bad Parity.** Set to generate bad primary cache tag parity on fills. Cleared by reset.
DC_16K	<12>	W,0	**Select 16-Kbyte D-Cache.** Set to select 16-Kbyte D-cache. Clear to select 8-Kbyte D-cache. Cleared by reset.

KN7AB BIU Control Register (BIU_CTL)

Address Abox 18
Access W

The BIU_CTL IPR is a write-only register that controls the operating parameters of the BIU interface and the B-cache. PALcode writes to this register at initialization and keeps an image of the register which appears in error log entries and is readable by the user.

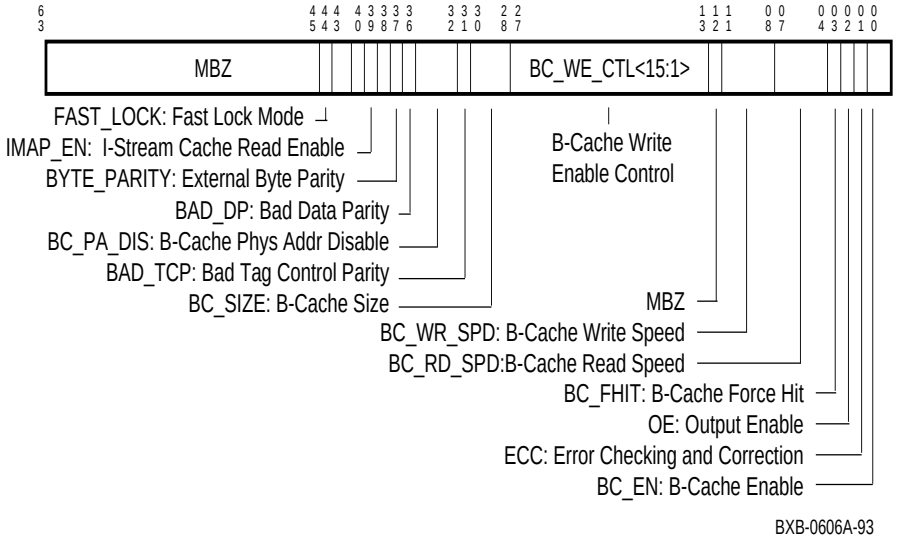


Table 2-4 KN7AB BIU_CTL IPR Bit Definitions, Revised

Name	Bit(s)	Type	Function
FAST_LOCK	<44>	W, 0	**Fast Lock Mode.** When set, FAST_LOCK mode operation is selected. This mode can only be used when BIU_CTL<2> is also set, indicating that OE-mode B-cache RAMS are used. Cleared by reset.
IMAP_EN	<39>	W, 0	**I-Stream Cache Read Enable**. Set to allow dMapWe_h<1:0> to assert for I-stream backup cache reads. Cleared by reset.
BYTE_PARITY	<37>	W, 0	**External Byte Parity.** If set when BIU_CTL<ECC> is clear, external byte parity is selected. When BIU_CTL<ECC> is set, this bit is ignored. Cleared by reset.

Section 3

Service Information

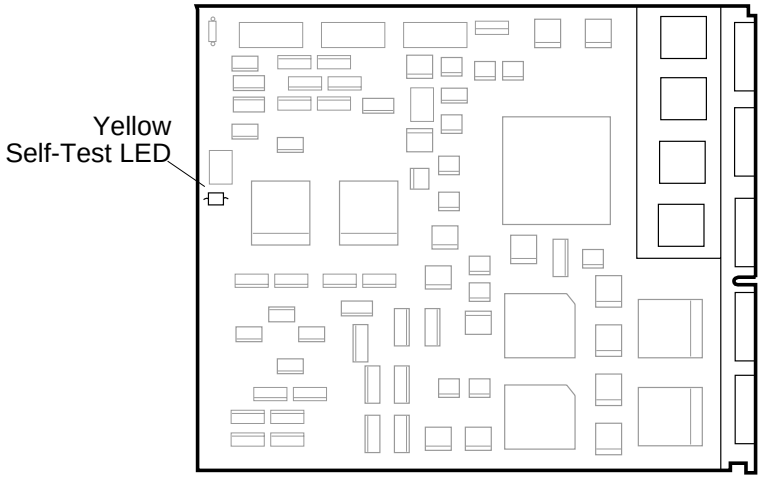
Information covered includes:

- KFMSB Adapter
- MS7AA-FA Memory Module
- Power Requirements for Options

3.1 KFMSB Adapter

DEC 7000/10000 systems now support the KFMSB adapter, which provides the XMI interface to DSSI buses. Each KFMSB supports two DSSI buses. The KFMSB has a diagnostic LED and reports status to the system self-test display.

Figure 3-1 KFMSB Module



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With the KFMSB adapter it is now possible to upgrade a VAX 7000/10000 system with a DSSI subsystem to a DEC 7000/10000 system with a DSSI subsystem.

Table 3-1 KFMSB Kit Contents

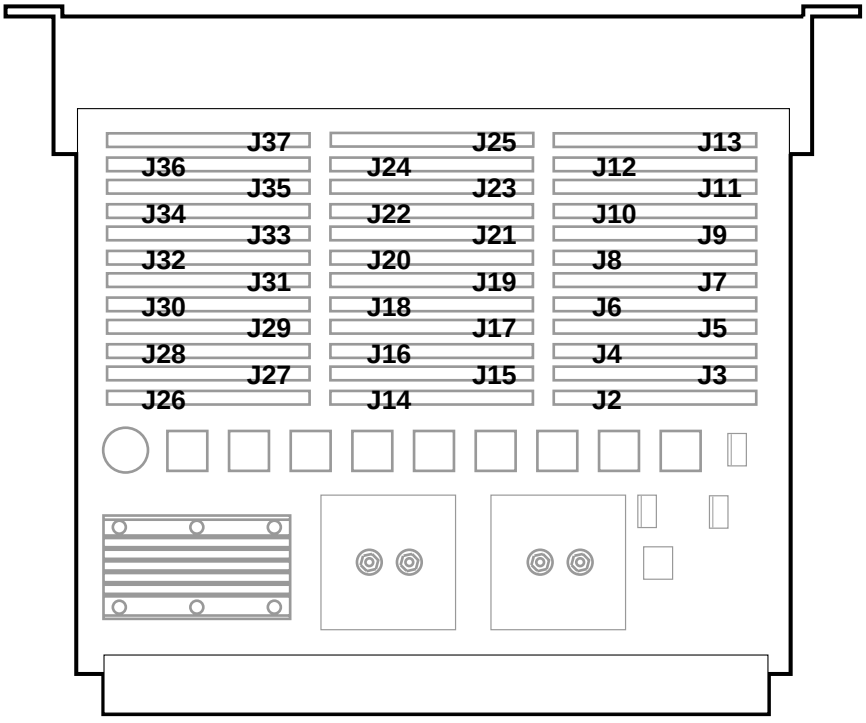
Option Number	Description
KFMSB-AA	Includes the KFMSB XMI module that supports DSSI systems in DEC 7000 and 10000 (AXP) systems and an installation guide (EK-KFMSB-IN).
KFMSB-UA	The upgrade kit includes the KFMSB XMI module, the installation guide, **and** the KFMSB cabinet kit (CK-KFMSB-LB).

LFU now allows you to change the DSSI node number of a KFMSB adapter, using the **modify** command.

3.2 MS7AA-FA Memory Module

Restrictions on use of the 2-gigabyte memory module depend on the operating system.

Figure 3-2 MS7AA-FA 2-Gbyte Memory Showing J Connectors for SIMMs



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The MS7AA-FA memory module is the 2-gigabyte memory module for VAX 7000/10000 and DEC 7000/10000 systems. It is populated with 36 64-Mbyte single in-line memory modules (SIMMs).

Restrictions on its use depend on the operating system.

The following versions of console firmware are required to support the MS7AA-FA module:

- For VAX 7000 systems
  Version 3.2 with KA7AA modules
  Version 1.0 with KA7AB modules
- For DEC 7000 systems
  Version 3.2 with KN7AA modules
  Version 3.3 with KN7AB modules

For more information: Repair instructions can be found on TIMA. See:

MS7AA-FA Memory Module Service Guide **(EK-MS7AA-SV).**

3.3 Power Requirements for Options

Various options have been released since the introduction of the VAX 7000/10000 and DEC 7000/10000 systems.

Table 3-2 lists the power requirements for each option, needed in calculating the need for a second power regulator. Power requirements are measured in equivalent power units (EPUs). This information updates the information found in Table B-1 of the *Advanced Troubleshooting* manuals.

Table 3-2 Power Requirements for Options

Option	EPUs
DEFAA Futurebus+ to FDDI adapter	3
DWLVA VME adapter	3
KFMSB XMI SCSI controller	3
KZASA Futurebus+ FWD SCSI controller	3
KZMSA XMI SCSI controller	3
MS7AA-FA 2-Gbyte memory module	10
MS7BB 16-Mbyte battery backup memory module	10

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