VAX 7000
Technical Bulletin Number 4

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This document accompanies the release of the KA7AC CPU module used in VAX 7000/10000 systems.

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Contents

Preface

Intended Audience

This document is written for system managers and service engineers.

Document Purpose

This technical bulletin provides information to update the VAX 7000/10000 documentation set. Since the original documentation set was published, we have issued one other Technical Bulletin that is a part of the documentation set:

- *DEC 7000 AXP VAX 7000 Technical Bulletin Number 3*
  EK–70TBA–T3

If you have an Internet account, you may mail us your comments on VAX 7000/DEC 7000 hardware documentation. Please mail your comments, suggestions, and corrections to **msbdoc@lando.enet.dec.com.** *We will reply to all comments. Digital values your input.*

Section 1

Installation

The KN7AC processor modules can be used to upgrade VAX 7000/10000 systems.

Sections include:

- Changes
- System Upgrades

1.1 Changes

VAX systems using KA7AC modules are currently supported by OpenVMS VAX Version 6.1 or later.

VAX Systems

The NV5 CPU chip on the KA7AC module provides improved performance over the NVAX and NVAX+ chips. The CPU chip is implemented in CMOS-5 technology. The chip speed of the KA7AC NV5 chip is 170.9 MHz compared with the chip speed of 137.5 on the KA7AB module and 91 MHz for the KA7AA NVAX+ chip.

One internal processor register has changed: the BIU Control Register.

Console Revision Requirements

KA7AC —V4.1 or later console is required.

1.2 System Upgrades

Upgrades can be of various types. Modules must be returned when the upgrade replaces the current CPU modules.

Upgrades can be of the following types:

- Upgrading from KA7AA or KA7AB modules to KA7AC modules
- Adding a KA7AC to an existing VAX system with KA7AC modules

Complete installation instructions are packaged with each CPU module.

Section 2

User Information

Changes to registers:

- KA7AC BIU Control Register

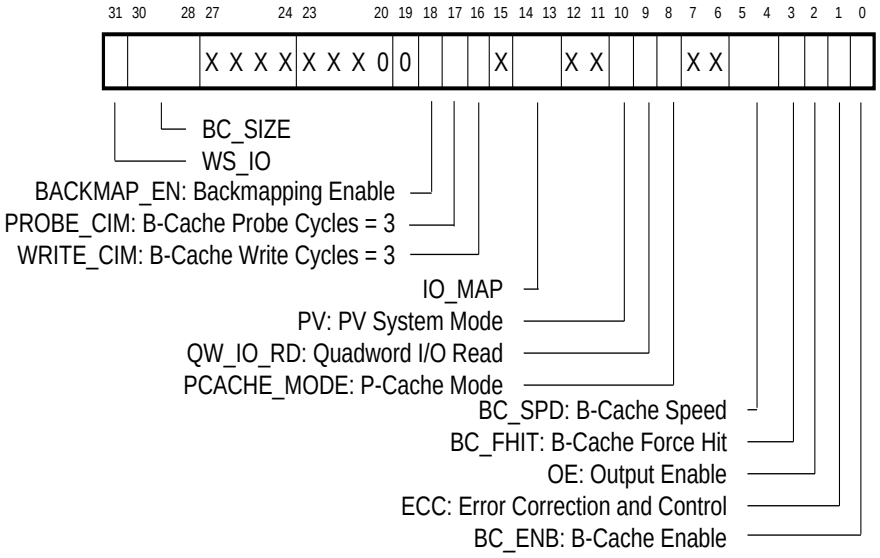
2.1 Registers

The following register information updates that given in the KA7AA CPU Technical Manual. The registers described are on-chip registers.

KA7AC BIU Control Register (BIU_CTL)

Address 00A0
Access R/W

The BIU_CTL register controls certain operations and parameters related to the P-cache, B-cache, and I/O mapping. This register reads the complement of its contents.



NOTE: X bits read values from DIAG_CTL.
This register reads inverted.

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Table 2-1 KA7AC BIU_CTL Register Bit Definitions, Revised

Name	Bit(s)	Type	Function
BACKMAP_EN	<18>	R/W, 0	**Backmap Enable.** Controls whether internal IRead aborts, which have been backmapped, generate invalidates to the P-cache. The console program sets this bit to 1.
PROBE_CIM	<17>	R/W, 0	**Probe Cache Cycle Injection Mode.** Controls the number of CPU cycles for all B-cache probes when set. The console program sets this bit to 1, which allows all B-cache probe cycles to increase from 2 to 3 CPU cycles.
WRITE_CIM	<16>	R/W, 0	**Write Cache Cycle Injection Mode.** Controls the number of CPU cycles for all B-cache writes when set. The console program sets this bit to 1, which increases the assertion duration on the dataWE_h<3:0> and tagCtWE_h pins from 2 to 3 CPU cycles.