EY-4818E-PP-0001

VAX 8600 TRAINING PRINT SET

Prepared by Educational Services
of
Digital Equipment Corporation

First Edition, January 1986

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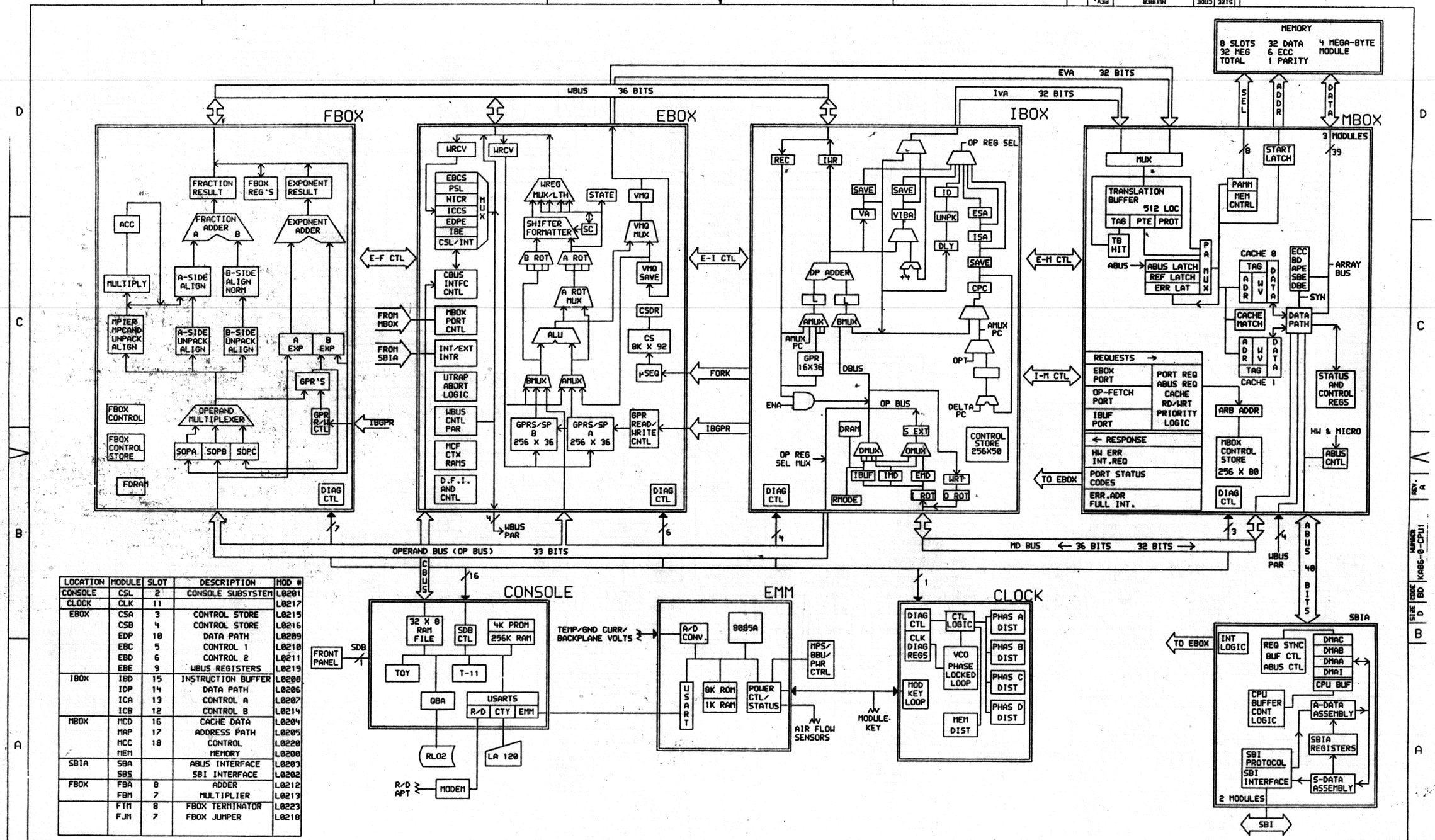


LOCATION	MODULE	SLOT	DESCRIPTION	MOD #
CONSOLE	CSL	2	CONSOLE SUBSYSTEM	L0201
CLOCK	CLK	11		L0217
EBOX	CSA	3	CONTROL STORE	L0215
	CSB	4	CONTROL STORE	L0216
	EDP	10	DATA PATH	L0209
	EBC	5	CONTROL 1	L0210
	EBD	6	CONTROL 2	L0211
	EBE	9	WBUS REGISTERS	L0219
IBOX	IBD	15	INSTRUCTION BUFFER	L0208
	IDP	14	DATA PATH	L0206
	ICA	13	CONTROL A	L0207
	ICB	12	CONTROL B	L0214
MBOX	MCD	16	CACHE DATA	L0204
	MAP	17	ADDRESS PATH	L0205
	MCC	18	CONTROL	L0220
	MEM		MEMORY	L0200
SBIA	SBA		ABUS INTERFACE	L0203
	SBS		SBI INTERFACE	L0202
FBOX	FBA	8	ADDER	L0212
	FBM	7	MULTIPLIER	L0213
	FTM	8	FBOX TERMINATOR	L0223
	FJM	7	FBOX JUMPER	L0218

REVISIONS		
CHK	CHANGE NO.	REV

digital

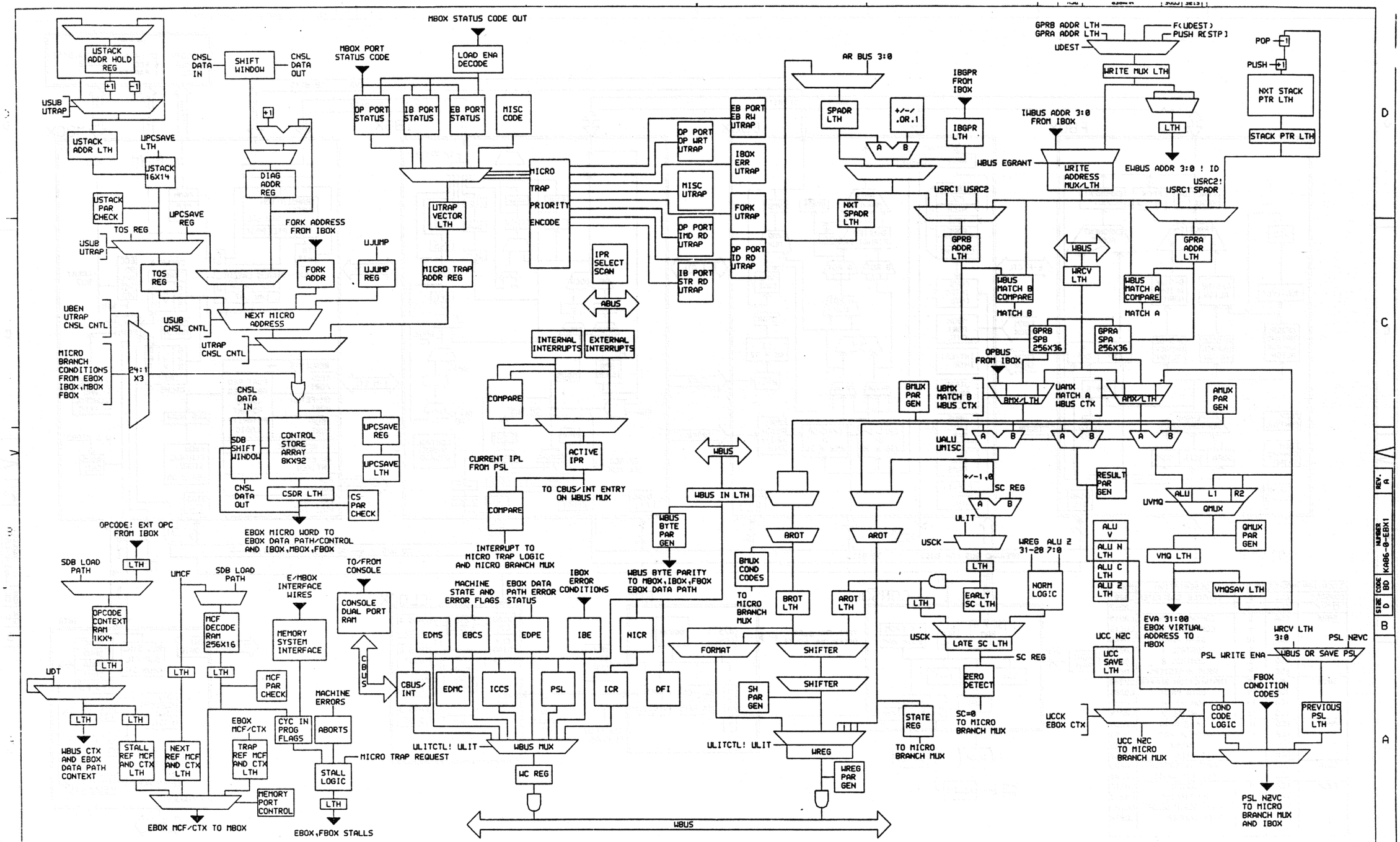
DRN. D.Tommy 10-SEP-84
CHK'D L.METZGER 10-SEP-84
ENG. W.WALTON 10-SEP-84
BOARD LOCATION:
SHEET OF
NEXT HIGHER ASSEMBLY: D-DD-KA86-0

VENFG1:<EBOX.SPECS>SYS.DRW 18-SEP-84 10:34
FIRST USED ON OPTION/MODEL:

TITLE: VENUS CPU BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-CPU1	A

2190C



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. L.CHAVES	DATE 13-SEP-84	ENG. B.HILLIARD	DATE 13-SEP-84	TITLE: EBOX BLOCK DIAGRAM	
CHK'D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION:			
VENUS1:<EBOX.SPEC>MENUBOX.DAV 13-SEP-84 06:59		SHEET 1 OF 1			
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE D / CODE BD / NUMBER KA86-0-EBX1 / REV. A	

8 7 6 5 4 3 2 1

2191

HEX DIGIT
DEF.MIC/ULD NUMBER
PHYSICAL RAM BIT

NOTE!
LAST UPDATE MADE
ON 07/02/83

21		20		19		18		17		16		15		14		13		12		11		10		9		8		7	
84		83		80		79		76		75		72		71		68		67		64		63		60		59		56		55	
62	63	51	21	56	57	58	59	80	81	76	77	78	79	82	83	73	48	49	50	31	30	29	33	32	40	41	42	43	88	89	90	91
UCCSYNC00	UNODEST00	PAR01	PAR00	UMISC03	UMISC02	UMISC01	UMISC00	UDT01	UDT00	UCCK03	UCCK02	UCCK01	UCCK00	UFBOX01	UFBOX00	UMARK00	UMCF05	UMCF04	UMCF03	UMCF02	UMCF01	UMCF00	UOPSEL01	UOPSEL00	ULIT05	ULIT04	ULIT03	ULIT02	ULIT01	ULIT00	ULITCTL01	ULITCTL00
		UPAR 1:0		UMISC 3:0				UDT 1:0		UCCK 3:0				UFBOX 1:0		U MRK	UMCF 5:0						UOPSEL 1:0		ULIT 5:0						U LITCTL 1:0	

52	51	12	48	47	11	44	43	10	40	39	9	36	35	8	32	31	7	28
45	46	47	36	37	28	68	69	87	84	85	86	39	34	35	20	22	23	24	25	26	27	38
USCK02	USCK01	USCK00	UDEST05	UDEST04	UDEST03	UDEST02	UDEST01	UDEST00	USRC205	USRC204	USRC203	USRC202	USRC201	USRC200	USRC107	USRC106	USRC105	USRC104	USRC103	USRC102	USRC101	USRC100
USCK 2:0			UDEST 5:0						USRC2 5:0						USRC1 7:0							

UMISC

03	02	01	00	
0	0	0	0	NOP
0	0	0	1	CLEAR MEM/GPR WRITE AND IO READ FLAG
0	0	1	0	SET PSL<FPD>
0	0	1	1	CLEAR PSL<FPD>
0	1	0	0	ENABLE ERROR UTRAP
0	1	0	1	DISABLE ERROR UTRAP
0	1	1	0	SET STATE MODIFIED FLAG
0	1	1	1	CLEAR STATE MODIFIED FLAG
1	0	0	0	IBOX.SYNC , SYNC WITH IBOX AFTER FLUSH
1	0	0	1	ZERO EXTEND 1 BYTE AT ALU B,ZERO BITS<31:8>
1	0	1	0	ZERO EXTEND 2 BYTES AT ALU B,ZERO BITS<31:16>
1	0	1	1	ZERO EXTEND 3 BYTES AT ALU B,ZERO BITS<31:24>
1	1	0	0	CHECK FOR INTEGER OVERFLOW
1	1	0	1	UNWIND RLOG
1	1	1	0	ENABLE FORK TRAP
1	1	1	1	DIAGNOSTIC RESET TO EBOX AND MBOX INITIALIZE

UDT

01	00	
0	0	BYTE
0	1	WORD
1	0	LONG
1	1	USE INST DEPENDENT CONTEXT

UCCK

03	02	01	00	PSL.N	PSL.Z	PSL.V	PSL.C
0	0	0	0	ALU.N(UDT)	ALU.Z(UDT)	0	PSL.C
0	0	0	1	ALU.N(UDT)	ALU.Z(UDT)	ALU.V(UDT)	NOT.ALU.Z(UDT)
0	0	1	0	PSL.N	PSL.Z	PSL.V	PSL.C
0	0	1	1	ALU.N(UDT) .XOR. ALU.V(UDT)	ALU.Z(UDT)	0	NOT.ALU.C(UDT)
0	1	0	0	ALU.N(UDT)	ALU.Z(UDT)	0	0
0	1	0	1	ALU.N(UDT)	ALU.Z(UDT)	ALU.V(UDT)	ALU.C(UDT)
0	1	1	0	ALU.N(UDT)	ALU.Z(UDT)	ALU.V(UDT)	NOT.ALU.C(UDT)
0	1	1	1	PSL.N	PSL.Z	1	PSL.C
1	0	0	0	PSL.N	PSL.Z	NOT.ALU.Z(UDT)	PSL.C
1	0	0	1	PSL.N	PSL.Z	PSL.V	PSL.C
1	0	1	0	ALU.N(UDT)	ALU.Z(UDT)	ALU.V(UDT)	PSL.C
1	0	1	1	ALU.N(UDT)	ALU.Z(UDT) .AND. PSL.Z	PSL.V	PSL.C
1	1	0	0	LOAD THE BMX CONDITION CODES AND WRE6<31> BRANCH			
1	1	0	1	LOAD THE UCC CONDITION CODES FROM ALU RESULTS			
1	1	1	0	LOAD ALL THE MICRO CONDITION CODES (BOTH UCC AND BMX)			
1	1	1	1	LOAD THE PSL CONDITION CODES FROM THE F-BOX			

UFBOX

01	00	
0	0	NOP
0	1	CPSYNC
1	0	TRAP
1	1	TRAP AND SYNC

NODEST

00	
0	EBOX WBUS REQUEST
1	NOT EBOX WBUS REQUEST

UMARK

00	
0	NOP
1	MARK/BREAKPOINT

CCSYNC

00	
0	NOP
1	PSL COND. CODES VALID

UMCF

05	04	03	02	01	00	
0	0	0	0	0	0	READ.VA.SAV
0	0	0	0	0	1	READ.VIBA.SAV (CLR.RL.INTR)
0	0	0	0	1	0	READ.ESA (CLR.TRX.INTR)
0	0	0	0	1	1	READ.ID
0	0	0	1	0	0	READ.CPC (CLR.TTX.INTR)
0	0	0	1	0	1	READ.ISA
0	0	0	1	1	0	
0	0	0	1	1	1	CLR.INTR.EN
0	0	1	0	0	0	
0	0	1	0	0	1	E.DISPATCH.I
0	0	1	0	1	0	FUNC.ECO1
0	0	1	0	1	1	PROBE.READ
0	0	1	1	0	0	READ.MBOX.REG
0	0	1	1	0	1	READ.PTE.TAG
0	0	1	1	1	0	READ.PTE
0	0	1	1	1	1	SWEEP.CACHE
0	1	0	0	0	0	ECO1
0	1	0	0	0	1	ECO2
0	1	0	0	1	0	READ.DIAG.IOA
0	1	0	0	1	1	READ.V.WCHK
0	1	0	1	0	0	READ.ECO1
0	1	0	1	0	1	READ.V.LOCK.WCHK
0	1	0	1	1	0	READ.V.WCHK.NOROT
0	1	0	1	1	1	READ.V.RCHK.NOROT
0	1	1	0	0	0	READ.V.SEC.REF
0	1	1	0	0	1	READ.V.NOPAGE
0	1	1	0	1	0	READ.P
0	1	1	0	1	1	READ.V.RCHK
0	1	1	1	0	0	READ.V.NCHK
0	1	1	1	0	1	REQUEUE.IB.REF
0	1	1	1	1	0	REQUEUE.EB.NEXT.REF
0	1	1	1	1	1	REQUEUE.EB.TRAP.REF
1	0	0	0	0	0	STOP.OP.PORT
1	0	0	0	0	1	ENABLE.OP.PORT
1	0	0	0	1	0	CLEAR.SUSPEND.BIT
1	0	0	0	1	1	OP.WRITE
1	0	0	1	0	0	UTRAP.TO.IFORK
1	0	0	1	0	1	FLUSH.IB.WBUS&WO.CPC
1	0	0	1	1	0	FLUSH.IB.WBUS&LD.CPC
1	0	0	1	1	1	FLUSH.IB.CPC
1	0	1	0	0	0	EN.OP.WRITE.STALL
1	0	1	0	0	1	CLEAR.EB.STATUS
1	0	1	0	1	0	CLEAR.MBOX.ERR.REG
1	0	1	0	1	1	PROBE.WRITE
1	0	1	1	0	0	WRITE.MBOX.REG
1	0	1	1	0	1	CLEAR.TB.ENTRY
1	0	1	1	1	0	WRITE.PTE
1	0	1	1	1	1	CLEAR.CACHE
1	1	0	0	0	0	WRITE.EMD
1	1	0	0	0	1	ECO3
1	1	0	0	1	0	WRITE.DIAG.IOA
1	1	0	0	1	1	WRITE.V.WCHK
1	1	0	1	0	0	WRITE.V.WCHK
1	1	0	1	0	1	WRITE.V.UNLOCK
1	1	0	1	1	0	WRITE.V.STRING.SEC.REF
1	1	0	1	1	1	WRITE.ECO1
1	1	1	0	0	0	WRITE.V.SEC.REF
1	1	1	0	0	1	WRITE.V.NOPAGE
1	1	1	0	1	0	WRITE.P
1	1	1	0	1	1	WRITE.V.STRING
1	1	1	1	0	0	WRITE.V.NCHK
1	1	1	1	0	1	REQUEUE.OP.IBF
1	1	1	1	1	0	REQUEUE.OP.REF
1	1	1	1	1	1	REQUEUE.OP.NOPAGE

UOPSEL

01	00	
0	0	IB REG SELECTED BY UREGSEL UMCF<2:0>
0	1	EMD
1	0	BYTE BUFFER (# OF BYTES SELECTED BY UMISC<1:0>)
1	1	OPERAND

ULITCTL/ULIT

01	00	05	04	03	02	01	00	
0	0	0	0	0	0	0	0	SHIFT AMX ! BMX LEFT (SC) BITS
0	0	0	0	0	1	X	0	0	PASS SC REGISTER
0	0	0	0	1	X	X	0	0	PASS ALU (NO SHIFT)
0	0	0	1	0	0	0	0	1	SHIFT ALU LEFT 1, INPUT VMQ<31>
0	0	0	1	0	0	0	1	0	SHIFT ALU RIGHT 2, INPUT 00
0	0	0	1	X	0	0	1	1	SHIFT ALU RIGHT 1, INPUT 0
0	0	0	1	0	0	1	0	1	SHIFT ALU LEFT 1, INPUT UCC.N
0	0	0	1	0	1	1	1	0	SHIFT ALU RIGHT 2, INPUT 01
0	0	0	1	X	1	1	1	1	SHIFT ALU RIGHT 1, INPUT 1
0	0	0	1	1	0	0	0	1	SHIFT ALU LEFT 1, INPUT 0
0	0	0	1	1	0	1	1	0	SHIFT ALU RIGHT 2, INPUT 10
0	0	0	1	1	1	0	0	1	SHIFT ALU LEFT 1, INPUT 1
0	0	0	1	1	1	1	1	0	SHIFT ALU RIGHT 2, INPUT 11
0	0	1	0	0	0	0	0	0	NIBBLE SWAP (OR CVT2P)
0	0	1	0	0	1	C	0	0	BYTE SWAP
0	0	1	0	1	0	0	0	0	CVTPN
0	0	1	1	0	0	0	0	0	F FORMAT PACK+
0	0	1	1	0	1	0	0	0	F FORMAT PACK-
0	1	X	X	X	X	X	X	X	USE ULIT FIELD AS SHIFT COUNT;ROTATE LEFT 0 THROUGH 63 PLACES
1	0	1	X	X	X	X	X	X	USE THE ULIT FIELD<4:0> TO SELECT THE HARDWARE REGISTER TO BE WRITTEN OVER THE W BUS
1	0	0	X	X	X	X	X	X	USE THE ULIT FIELD<4:0> TO SELECT THE HARDWARE REGISTER TO BE READ OVER THE W BUS
1	1	0	X	X	X	X	X	X	USED FOR FBOX CONTROL IF ULIT<5>=0 THEN THE FBOX WILL ENABLE DATA ONTO THE WBUS (FBOX RESULT DATA)
1	1	1	X	X	X	X	X	X	USED FOR FBOX CONTROL IF ULIT<5>=1 THEN EBOX WILL ENABLE DATA ON WBUS TO BE GIVEN TO FBOX (FBOX OPER DATA)
1	1	1	X	X	X	X	X	X	IF UFBOX FIELD EQUAL TO TRAP OR TRAP AND SYNC, THEN USE ULIT<4:0> AS NEW PC FOR FBOX MICRO SEQUENCER

USCK

02	01	00	
0	0	0	DECREMENT SC REGISTER
0	0	1	INCREMENT SC REGISTER
0	1	0	LOAD SC FROM AR BUS
0	1	1	LOAD STATE FROM AR BUS
1	0	0	LOAD SC FROM NV1, OTHER BITS GET 0
1	0	1	LOAD SC FROM NV2, OTHER BITS UNAFFECTED
1	1	0	NOP
1	1	1	LOAD SC FROM ULIT<5:0>

UDEST

05	04	03	02	01	00	LOGICAL REG. DEST.	PHYSICAL REG. DEST.	RAM A ADDRESS SOURCE	RAM B ADDRESS SOURCE
MODE 2	0	0	X	0	0	0	R0 THRU R15 OR T0 THRU T1F	0!USRC1<3:0>!UDEST<1:0>	USRC2<5:2> ! SPADR<3:0>	USRC1<7:4> ! SPADR<3:0>
	0	0	X	0	0	1				
	0	0	X	0	1	0				
	0	0	X	0	1	1				
	0	0	X	1	0	0	PUSH R<STP>	F ! STP<3:0>		
	0	0	X	1	0	1	NO.DEST	N/A		
	0	0	X	1	1	0	READ A	USRC2<5:2>!SPADR<3:0>		
	0	0	X	1	1	1	READ B	USRC1<7:4>!SPADR<3:0>		
MODE 1	0	1	X	0	0	0	T0	10	USRC2<5:2> ! SPADR<3:0>	USRC1<7:0>
	0	1	X	0	0	1	T1	11		
	0	1	X	0	1	0	T2	12		
	0	1	X	0	1	1	T3	13		
	0	1	X	1	0	0	PUSH R<STP>	F ! STP<3:0>		
	0	1	X	1	0	1	NO.DEST	N/A		
	0	1	X	1	1	0	READ A	USRC2<5:2>!SPADR<3:0>		
	0	1	X	1	1	1	READ B	USRC1<7:0>		
MODE 0	1	0	0	0	0	0	T0	10	USRC1<7:0>	USRC2<5:0>
	1	0	0	0	0	1	T1	11		
	1	0	0	0	1	0	T2	12		
	1	0	0	0	1	1	T3	13		
	1	0	0	1	0	0	T4	14		
	1	0	0	1	0	1	T5	15		
	1	0	0	1	1	0	T6	16		
	1	0	0	1	1	1	T7	17		
	1	0	1	0	0	0	T8	18		
	1	0	1	0	0	1	T9	19		
	1	0	1	0	1	0	TA	1A		
	1	0	1	0	1	1	TB	1B		
	1	0	1	1	0	0	TC	1C		
	1	0	1	1	0	1	TD	1D		
	1	0	1	1	1	0	TE	1E		
	1	0	1	1	1	1	TF	1F		
	1	1	0	0	0	0	T10	20		
	1	1	0	0	0	1	T11	21		
	1	1	0	0	1	0	T12	22		
	1	1	0	0	1	1	T13	23		
	1	1	0	1	0	0	T14	24		
	1	1	0	1	0	1	PUSH R<STP>	F ! STP<3:0>		
	1	1	0	1	1	0	READ A	USRC1<7:0>		
	1	1	0	1	1	1	READ B	0 ! USRC2<5:0>		
	1	1	1	0	0	0	R0	0		
	1	1	1	0	0	1	R1	1		
	1	1	1	0	1	0	R2	2		
	1	1	1	0	1	1	R3	3		
	1	1	1	1	0	0	R4	4		
	1	1	1	1	0	1	R5	5		
	1	1	1	1	1	0	R14	E		
	1	1	1	1	1	1	NO.DEST	N/A		

IF UDEST<5>=0 THEN USE UDEST<3> WITH USRC2<1:0>.
TO DECODE ONE OF THE BELOW FUNCTIONS FOR SPADR OR STP

UDEST 5:0						USRC2 1:0		
05	04	03	02	01	00	01	00	
0	X	0	X	X	X	0	0	INCREMENT SPADR
0	X	0	X	X	X	0	1	DECREMENT SPADR
0	X	0	X	X	X	1	0	LOAD SPADR FROM ALU<3:0>
0	X	0	X	X	X	1	1	OR 1 INTO SPADR<0>
0	X	1	X	X	X	0	0	NOP
0	X	1	X	X	X	0	1	LOAD SPADR FROM IBGPR
0	X	1	X	X	X	1	0	INCREMENT STP (STACK POINTER)
0	X	1	X	X	X	1	1	READ REF!STP<3:0>] AND DECREMENT STP, POP STACK

REVISIONS		
CHK	CHANGE NO.	REV

DRN. A. OPPENHEIM	DATE 21-SEP-84	ENG. B.HILLIARD	DATE 21-SEP-84
CHK'D L.METZGER	DATE 21-SEP-84	BOARD LOCATION:	
VENGG1::<EBOX.SPECS>UWORD1.DAV 21-SEP-84 08:57		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:		D-DD-KA86-0	

TITLE: UWORD PAGE 1

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-EBX2	A

HEX DIGIT 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0

DEF.MIC/ULD NUMBER
PHYSICAL RAM BIT NUMBER

28	27	24	23	20	19	16	15	12	11	08	07	04	03	00
64	66	67	65	44	70	71	72	74	75	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
USMI 0	UVMQK 1:0	UBMX	UAMX	UALU 4:0					UBEN 4:0					USUB 1:0		UJUMP 12:0													

USMI

00	
0	START OF NEW MACRO INSTRUCTION
1	NOT START OF NEW MACRO INSTRUCTION

UVMQK

01	00	
0	0	HOLD
0	1	LOAD ALU RESULT
1	0	SHIFT LEFT 1,SHIFT IN ALU.C.31
1	1	SHIFT RIGHT 2,SHIFT IN ALU<1:0>

UBMX

00	
0	RAM B SELECT
1	OPBUS SELECT

UAMX

00	
0	RAM A SELECT
1	VMQ SELECT

UALU

04	03	02	01	00	OPERATION	CARRY/BORROW
					LOGICAL	
0	0	0	0	0	A.AND.B	X
0	0	0	0	1	A.XOR.B	X
0	0	0	1	0	B	X
0	0	0	1	1	A.OR.B	X
0	0	1	0	0	A.AND.(NOT.B)	X
0	0	1	0	1	A	X
0	0	1	1	1	(NOT.A).AND.B	X
					ARITHMETIC	
0	0	1	1	0	DIVIDE A+/-B	UCC.C=0/1
0	1	0	0	0	A+4	+0
0	1	0	0	1	A-4	-0
0	1	0	1	0	A+B KORRECT (BCD)	
0	1	0	1	1	LOAD.CONFIG	
0	1	1	0	0	A-B	-1
0	1	1	0	1	A-B	-0
0	1	1	1	0	A-B	- NOT UCC.C
0	1	1	1	1	A-B	-PSL.C
1	0	0	0	0	A+B	+0
1	0	0	0	1	A+B	+1
1	0	0	1	0	A+B	+UCC.C
1	0	0	1	1	A+B	+PSL.C
1	0	1	0	0	B-A	-1
1	0	1	0	1	B-A	-0
1	0	1	1	0	B-A	- NOT UCC.C
1	0	1	1	1	B-A	-PSL.C
1	1	0	0	0	A+B (BCD)	+0
1	1	0	0	1	A+B (BCD)	+1
1	1	0	1	0	A+B (BCD)	+UCC.C
1	1	0	1	1	A+B (BCD)	+PSL.C
1	1	1	0	0	A-B (BCD)	-1
1	1	1	0	1	A-B (BCD)	-0
1	1	1	1	0	A-B (BCD)	- NOT UCC.C
1	1	1	1	1	A-B (BCD)	-PSL.C

DIAG. MODE ONLY
ONLY IF "EDPE" AND STATE = 2

UBEN

04	03	02	01	00	UPC <2>	UPC <1>	UPC <0>
0	0	0	0	0	0	0	0
0	0	0	0	1	UCC.N	UCC.2	UCC.C
0	0	0	1	0	0	UCC.2	0
0	0	0	1	0	DIAG1	UCC.2	DIAG0
0	0	0	1	0	A.RAM.PE	0	0.RAM.PE
0	0	0	1	1	SC.EQ.0	0	UCC.C
0	0	1	0	0	PSL.N	PSL.2	PSL.C
0	0	1	0	1	ESA.VALID	ISA.VALID	UNWIND.DONE
0	0	1	1	0	OPCODE2	OPCODE1	OPCODE0
0	0	1	1	1	OPCODE4		EXT.OPCODE
0	1	0	0	0	STATE2	UCC.N	DECIMAL.SIGN
0	1	0	0	1	IBUF.VA	NEXT.EB.VALID	TRAP.OP.WCHK
0	1	0	1	0	SC.EQ.0	VMQ1	VMQ0
0	1	0	1	1	PSL.IS	PSL.FPD	KERNEL
0	1	1	0	0	CPC.VALID	PSL.CM	INTERRUPT
0	1	1	0	1	STATE2	STATE1	STATE0
0	1	1	1	0	STATE5	STATE4	STATE3
0	1	1	1	1	STATE7	STATE6	WREG31
1	0	0	0	0	TRAP.EB.WCHK	TB.CHECK1	TB.CHECK0
1	0	0	0	1	0	VMQ31	PSL.V
1	0	0	1	0	SC.EQ.0	UCC.2	30.LE.BMX.LE.39
1	0	0	1	1	BMX15	UCC.2	FL.EXP=0
1	0	1	0	0	FBOX2	FBOX CARRY	FBOX ENABLED
1	0	1	0	1	TRAP.EB.WRITE	NEXT.EB.WRITE	TRAP.EB.WORD.OR.BYTE
1	0	1	1	0	TRAP.OP.WRITE		NEXT.OP.WR
1	0	1	1	1			
1	1	0	0	0			
1	1	0	0	1			
1	1	0	1	0			
1	1	0	1	1			
1	1	1	0	0			
1	1	1	0	1			
1	1	1	1	0			
** 1	1	1	1	1	0	0	0

** GENERATES THE SIGNAL IRD

USUB

01	00	
0	0	JUMP
0	1	RETURN
1	0	FORK
1	1	CALL SUB.

UJUMP

12	11	10	09	08	07	06	05	04	03	02	01	00	
X	X	X	X	X	X	X	X	X	X	X	X	X	THIS FIELD SPECIFIES THE NEXT MICRO ADDRESS FOR E-BOX MICRO SEQUENCER

NOTES

RAM A	EBOX GPR A OR SCRATCH PAD A
RAM B	EBOX GPR B OR SCRATCH PAD B
AR BUS	A OPERAND OR ALU RESULT BUS
ECO#	FOR FUTURE USE

REVISIONS

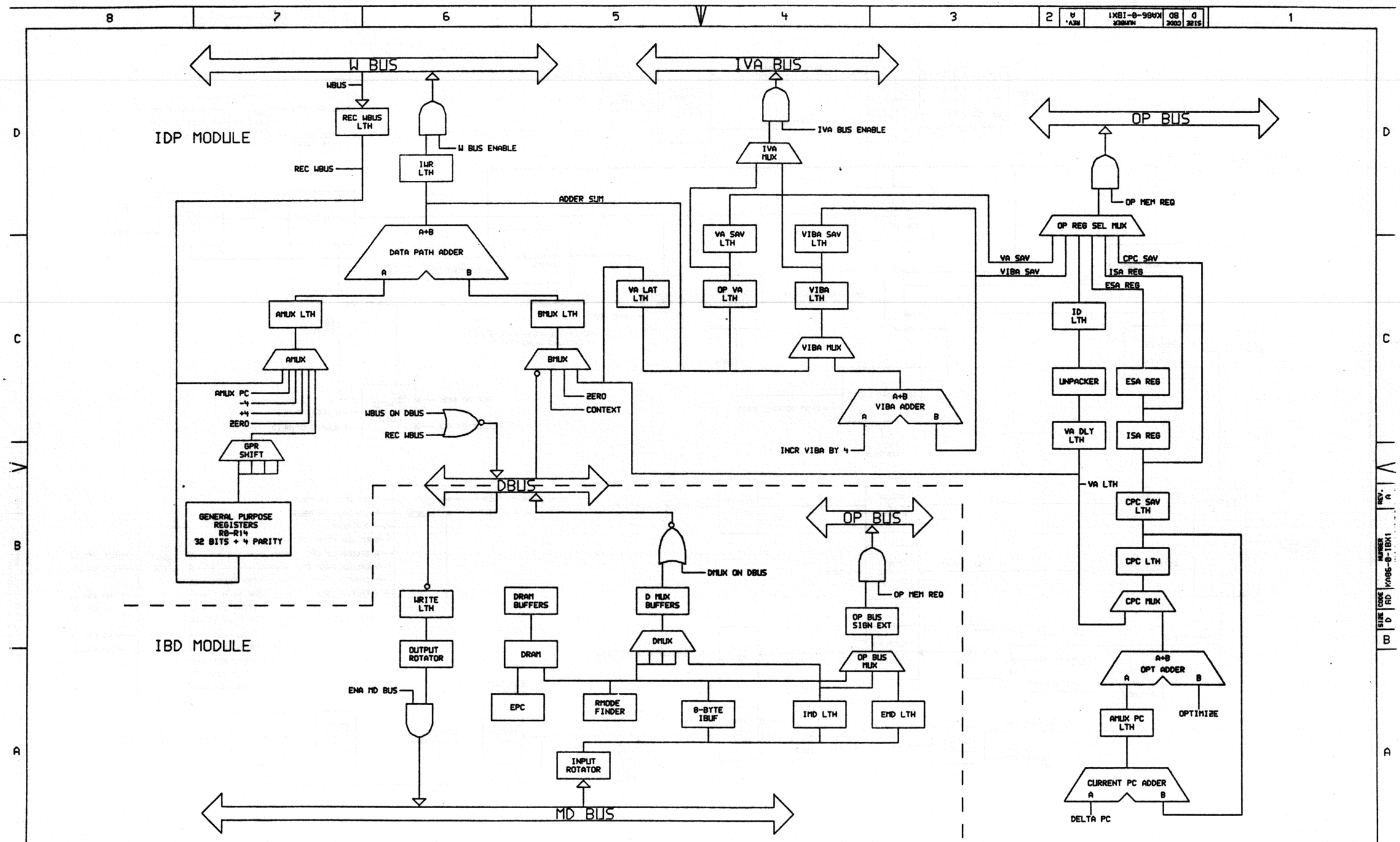
CHK	CHANGE NO.	REV

digital

DRN. A. OPPENHEIM — DATE 12-SEP-84 — ENG. B.HILLIARD — DATE 12-SEP-84
CHK'D L.METZGER — DATE 13-SEP-84
BOARD LOCATION:
SHEET 1 OF 1
VENB01:<EBOX.SPECS>UWORD8.DAM 13-SEP-84 07:14
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
D-DD-KA86-0

TITLE: UWORD PAGE 2

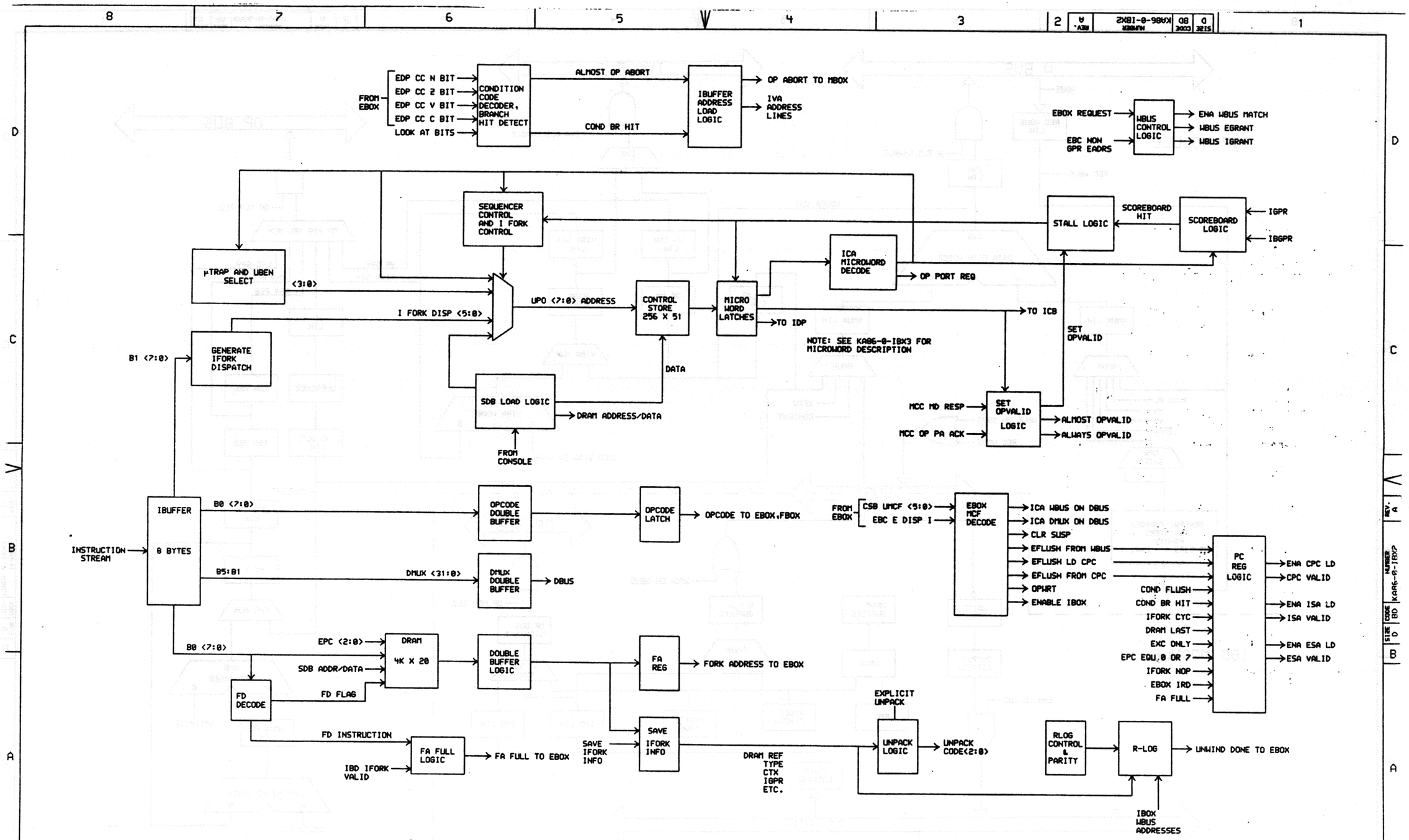
SIZE	CODE	NUMBER	REV.
D	CS	KA86-0-EBX3	A



REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. R.DAME	DATE 19-SEP-84	ENG. F.MCKEEN	DATE 19-SEP-84	TITLE: VENUS IBOX DATA PATHS
	CHK'D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION: SHEET 1 OF 1		
VENUS1::<IBOX.BD-SUB>IBX1BD.DRW 18-SEP-84 13:23			NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE D / CODE BD / NUMBER KA86-0-IBX1 / REV. A
FIRST USED ON OPTION/MODEL:					

2194



REVISIONS		
CHK	CHANGE NO.	REV

DRN C.CAIA22I	DATE 03-OCT-84	ENG F.MCKEEN	DATE 03-OCT-84	TITLE: VENUS IBOX CONTROL PATHS	
CHK D. L.METZGER	DATE 03-OCT-84	BOARD LOCATION: SHEET 1 OF 1			
VENI01:<IBOX.BD-SUB>IBX2BD.DRW 02-OCT-84 11:55		NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE D / CODE BD / NUMBER KA86-0-IBX2	REV. A
FIRST USED ON OPTION/MODEL:					

2195

UPAR	UMISC2			MARK	DIAG UNS-TALL	IB HOLD	UNS-TALL	CYCLE ID		UMISC				MCF				UNPACK CTL		OPVALID		REG MODE	WBUS REQ	GPR SEL			CTX CTL			BMUX SEL			AMUX SEL			UTRAP CTL		IFORK			UBEN		NEXT								
50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

UPAR<0:0> ODD PARITY GENERATED ON MICROWORD

UMISC2<2:0> MISCELLANEOUS 2
- 0 = NOP
- 1 = INDEX.IMM
- 2 = ENA.OPBUS.PARITY
- 3 = UNUSED
- 4 = FORCE.SET.SB.VALID
- 5 = INHIBIT.SET.SB.VALID
- 6 = FORCE.SET.SB.ENA.OPBUS.PARITY
- 7 = UTRAP.CIP

MARK<0:0> STOP CPU CLOCKS IN NEXT MICROCYCLE

DIAG UNSTALL<0:0> OVERRIDE ALL IBOX STALL TERMS

IB HOLD<0:0> FREEZE IBUFFER FOR DIAGNOSTICS

UNSTALL<0:0> OVERRIDE IB.STOP AND SUSPEND STALL

CYCLE ID<1:0>
- 0 = NON-IFORK CYCLE
- 1 = INDEX IFORK ENTRY [R]
- 2 = BASE OPERAND ADDRESS (BOA) ENTRY
- 3 = IFORK ENTRY AND -(BOA + [R])

UMISC<3:0> MISCELLANEOUS
- 0 = NOP
- 1 = STALL UNTIL EBOX OP.WRITE COMMAND
- 2 = IB.FLUSH.LD.CPC
- 3 = IB.FLUSH
- 4 = COND.BRANCH
- 5 = IB.FLUSH.COND
- 6 = READ.IMD
- 7 = INH.SB.CHECK
- 8 = RAF RESERVED ADDRESSING MODE
- 9 = DIAG.DONE
- A = DIAG.RESET
- B = BMUX.CHK.CTX
- C = POP STACK
- D = CLEAR CPC VALID ; FOR FLUSH AND BRANCH
- E = COND.FA.OP.MEM.REQ
- F = FA.OP.MEM.REQ

MCF<3:0> MEMORY CONTROL FIELD
- 0 = READ.RCHK IF DRAM MEM EQUALS READ
  READ.WCHK IF DRAM MEM EQUALS MODIFY
- 1 = NO OP-PORT MEMORY REQUEST
- 2 = WRITE+V+NOPAGE
- 3 = WRITE+V+NOPAGE.2ND
- 4 =
- 5 = WRITE+V+WCHK
- 6 =
- 7 =
- 8 = READ+V+WCHK
- 9 =
- A = READ+V+RCHK
- B = READ+V+RCHK.2ND
- C = READ+V+NOPAGE
- D = READ+V+NOPAGE.2ND
- E = IB.FILL.OP
- F = IB.FILL.IBF

UNPACK CTL<1:0> UNPACKER CONTROL
- 0 = NOP
- 1 = SIGN EXTEND IF -ASRC
- 2 = UNPACK AS SHORT LITERAL ACCORDING TO DRAM CTX AND TYPE FIELDS.
- 3 = UNUSED

OPVALID<1:0> OPERAND VALID
- 0 = NOP
- 1 = SET OPVALID IF ((READ+MODIFY+VSRC)*RMODE)+ -(ASRC+RMODE)
- 2 = SET OPVALID IF ASRC+((READ+MODIFY)*ALIGNED)
- 3 = SET OPVALID UNCONDITIONALLY

REG MODE<0:0> REGISTER MODE
- 0 = INDICATES THAT THIS IS NOT RN SPECIFIER
- 1 = INDICATES RN SPECIFIER

WBUSREQ<0:0> WBUS REQUEST
- 0 = RLOG ENTRY IS PUSHED IF THIS IS FIRST IFORK FOR THIS OPCODE. WBUS IS CONDITIONALLY REQUESTED IF DOING AN UNWIND.GPR SEL=3
- 1 = RLOG ENTRY IS PUSHED WITH VALID GPR NUMBER AND CONTEXT ENTRY. WBUS IS REQUESTED.

GPR SEL<2:0> GENERAL PURPOSE REGISTER SELECT
- 0 = GPR ADDRESS FROM IBUF ISTREAM <B1>
- 1 = INDEX REGISTER IS BEING ADDRESSED BY A SAVED INDEX REGISTER NUMBER.
- 2 = LAST GPR ADDRESS PLUS 1.
- 3 = GPR ADDRESS IS PREVIOUS GPR ADDRESS.
- 4 = RLOG+UNWIND
- 5 = GPR ADDRESS <3:2> <--- CTX CTL<1:0>
  GPR ADDRESS <1:0> <--- UNPACK.CTL<1:0>
- 6-7 = UNUSED

CTX CTL<2:0> CONTEXT CONTROL

	ADDER CTX	MEM CTX	RLOG CTX ENTRY
0	DRAM CTX	DRAM CTX	DRAM CTX
1	4	4	4
2			
3	+/-RLOG CTX	X	X
4	-DRAM CTX	DRAM CTX	-DRAM CTX
5	-4	4	X
6			
7			

X = UNDEFINED

BMX SEL<2:0> BMUX SELECTION
- 0 = ZERO
- 1 = VA
- 2 = ADDER CTX AS DEFINED BY CTX CTL
- 3 = UNUSED
- 4 = DMX.IBF
- 5 = DMX.IMD
- 6 = CPC ; USED FOR STRING CONTINUED FLUSHES.
- 7 = HOLD VA ; INHIBIT VA CLOCKING. NOT A BMUX SEL FUNCTION.

AMUX SEL<2:0> AMUX SELECTION
- 0 = ZERO
- 1 = AMUX PC
- 2 = +4
- 3 = -4
- 4 = GPR, IF WBUS MATCH REPLACE GPR DATA WITH WBUS DATA.
- 5 = GPR (LEFT SHIFT 1)
- 6 = GPR (LEFT SHIFT 2)
- 7 = WBUS
- 4-6 = ENABLE ISTALL IF SCOREBOARD HIT.
- 5-6 = ENABLE ISTALL IF WBUS MATCH.

UTRAP CTL<1:0> MICRO-TRAP CONTROL
- 0 = INHIBIT MICRO-TRAP DUE TO UNALIGNMENT.
- 1 = MICRO-TRAP NEXT CYCLE FOR UNALIGNED INDIRECT FETCH.
- 2 = MICRO-TRAP FOR UNALIGNED (RN) OR ANY OTHER UNALIGNED OPERAND.

IFORK CTL<2:0> IFORK CONTROL
- 0 = DO NOT IFORK
- 1 = IFORK IF ASRC+(READ*(BWL))
- 2 = IFORK IF VSRC+WRITE+((READ+MODIFY)*(BWL))
- 3 = IFORK IF READ*(BWL)
- 4 = IFORK IF QUAD
- 5 = IFORK IF EBOX UMCF EQUALS 24
- 6 = UNCONDITIONAL IFORK
- 7 = UNUSED

UBEN<1:0> MICRO-BRANCH ENABLE

	UBEN MUX 3	UBEN MUX 2	UBEN MUX 1	UBEN MUX 0
0	0	0	0	0
1	0	QUAD+OCTA	DRAM MEM 1	DRAM MEM 0
2	RLOG FIRST	DRAM CTX 2	DRAM CTX 1	DRAM CTX 0
3	0	0	0	0

NA<7:0> NEXT ADDRESS

REVISIONS		
CHK	CHANGE NO.	REV

DRN. L.MELLO	DATE 19-SEP-84	ENG. E.HANSON	DATE 19-SEP-84
CHK D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION: SHEET 1 OF 1	
VENTA1:<TROX.BD-SUB>IBXMB.DAV 18-SEP-84 10:27		NEXT HIGHER ASSEMBLY: D-DD-KA86-0	
FIRST USED ON OPTION/MODEL:			

TITLE: IBOX MICROWORD

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-IBX3	A

CTX			TYPE		REF		CTL		SUSP	BDEST	LAST	PAR	FPA	ADRS					
19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00

CTX<2:0>
- 0 = BYTE
- 1 = WORD (2 BYTES)
- 2 = LONG (4 BYTES)
- 3 = QUAD (8 BYTES)
- 4 = OCTA (16 BYTES)
- 5:7 = UNPREDICTABLE

TYPE<1:0>
- 0 = INTEGER, ASOURCE
- 1 = FLOATING, F, D, OR H
- 2 = G-FLOAT
- 3 = VSOURSE

REF<1:0>

	ACCESS CHECK ON READ	WRITE
0 = ASOURCE	--	--
0 = VSOURCE	--	--
1 = READ	READ	--
2 = WRITE	--	WRITE
3 = MODIFY	WRITE	WRITE

CTL<1:0>
- 0 = EXECUTE
- 1 = SINGLE
- 2 = OPT-TWO
- 3 = OPT-TWO & EXECUTE

SUSP<0:0>
- 0 =
- 1 = SUSPEND ADDRESS CACULATION

BDEST<0:0>
- 0 = NEXT BYTE AFTER THIS SPECIFIER IS A MODE-REGISTER SPECIFIER OR NEW OPCODE.
- 1 = NEXT BYTE AFTER THIS SPECIFIER IS A BRANCH DISPLACEMENT.

LAST<0:0>
- 0 =
- 1 = LAST ENTRY FOR THIS INSTRUCTION

PAR<0:0>
- X = ODD PARITY BIT

FPA<0:0>
- 0 =
- 1 = FPA MAY OVERRIDE THE EBOX FOR THE SPECIFIER

ADRS<5:0>
- X = BASIC FORK ADDRESS

FORK ADDRESSES BASED ON CTL FIELD

==CTL==	07	06	05	04	03	02	01	00
EXECUTE	0	DRAM<FPA>=FEN OR -DRAM<FPA>	DRAM ADRS <05:00>					
SINGLE ====	1	DRAM<FPA>=FEN OR -DRAM<FPA>	DRAM ADRS<05:01>				DRAM ADRS<00> & RMODE & -BDEST	
OPT-TWO RMODE	1	DRAM<FPA>=FEN	DRAM ADRS<05> & B1=REGMODE	DRAM ADRS<04:00>				
OPT-TWO NOT RMODE	1	DRAM<FPA>=FEN	DRAM ADRS<05> & B1=REGMODE	DRAM TYPE<1:0>		DRAM CTX<2:0>		
OPT-TWO & EXEC RMODE	0	DRAM<FPA>=FEN	DRAM ADRS<05:01>				DRAM ADRS<00> OR RMODE	
OPT-TWO & EXEC NOT RMODE ==	0	DRAM<FPA>=FEN	DRAM ADRS<05> & B1=REGMODE	DRAM ADRS<04:00>				

== IF FORK ADDRESS BIT 5 (FA<05>) = 1 TURN OFF THE SCOREBOARD.

=== IF FORK ADDRESS BIT 0 (FA<00>) = 1 TURN OFF THE SCOREBOARD.

TABLE 10
USE OF THE DRAM

EPC	NON FD INSTRUCTIONS	FD INSTRUCTIONS
0	1ST OPERAND	FPD DISPATCH
1	2ND OPERAND	1ST OPERAND
2	ETC..	2ND OPERAND
3	.	ETC..
4	.	.
5	.	.
6	.	.
7	FPD DISPATCH	NOT USED

NOTES: 1) THE OPERAND ENTRIES ARE THERE ONLY IF THE OPCODE HAS SUCH OPERANDS.
2) FPD => FIRST PART DONE. THE FPD DISPATCH FORKS THE EBOX TO THE FPD CODE FOR THE INSTRUCTION IT WAS DOING BEFORE IT WAS INTERRUPTED.

REVISIONS		
CHK	CHANGE NO.	REV

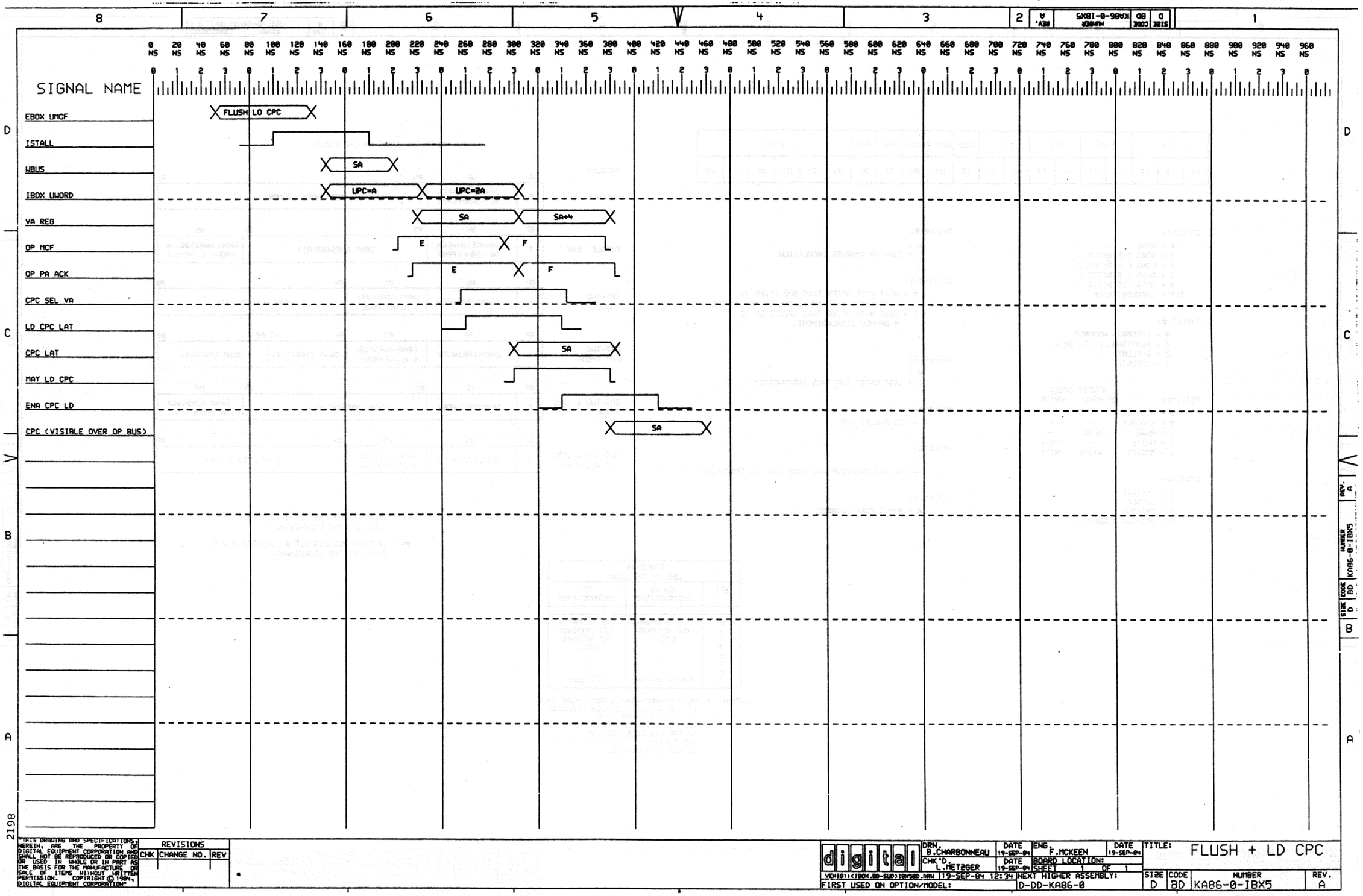
digital	DRN. L.MELLO	DATE 19-SEP-84	ENG. C.MAIMAN
	CHK D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION:
VENIG11:<IBOX.BD-SUD>IBOXED.DRA	18-SEP-84 10:30	NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:		D-DD-KA86-0	

DATE 19-SEP-84 | SHEET 1 OF 1

TITLE: IBOX DRAM FIELDS & FORK ADDRESS

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-IBX4	A

2197

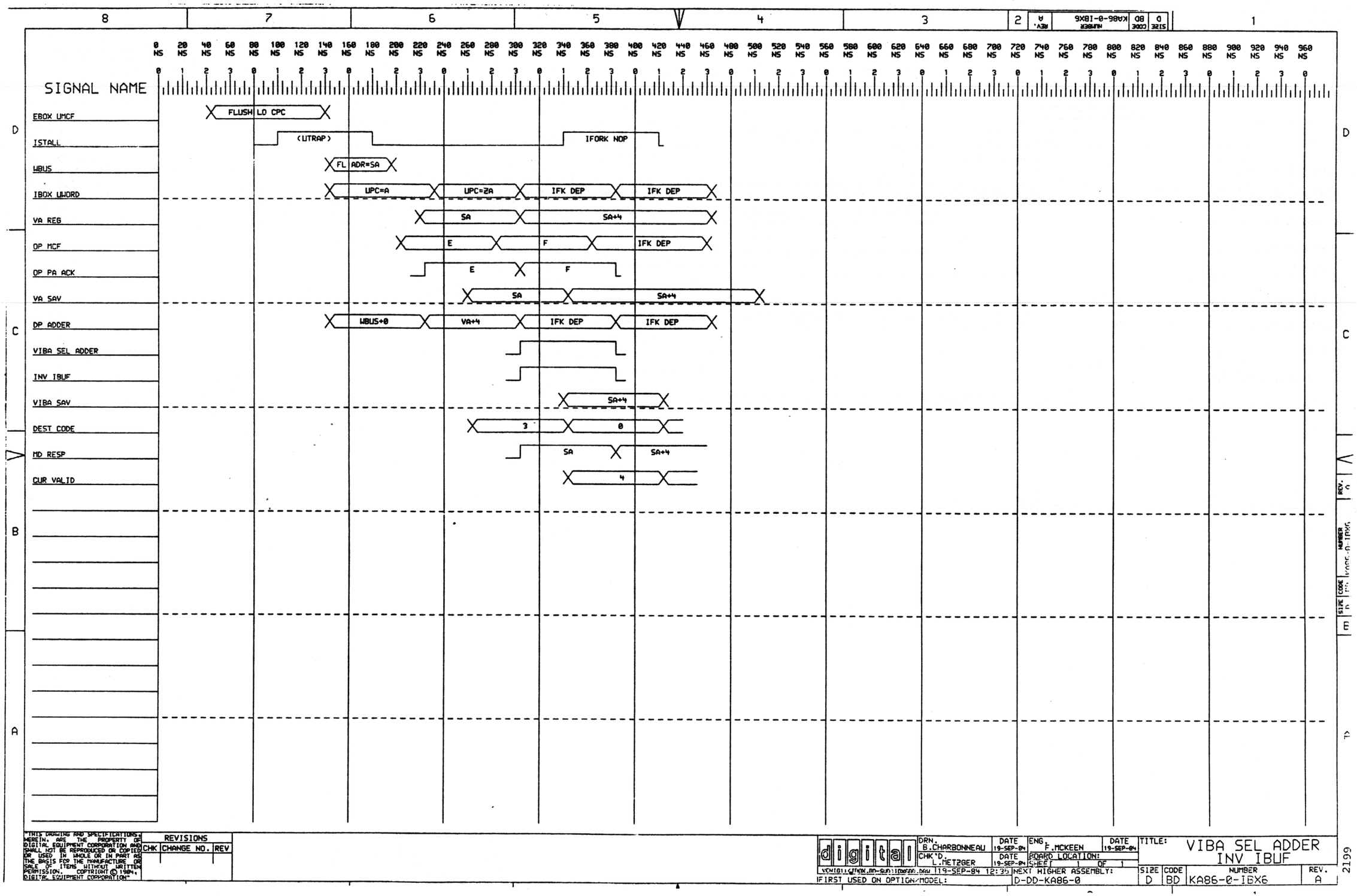


REVISIONS

CHK	CHANGE NO.	REV

DRN. B.CHARBONNEAU	DATE 19-SEP-84	ENG. F.MCKEEN	DATE 19-SEP-84	TITLE: FLUSH + LD CPC	
CHK'D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION: SHEET 1 OF 1			
VENIGI:<IBOX.BD-SUD>IBX5BD.DAV 19-SEP-84 12:34		NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE D / CODE BD / NUMBER KA86-0-IBX5	REV. A
FIRST USED ON OPTION/MODEL:					

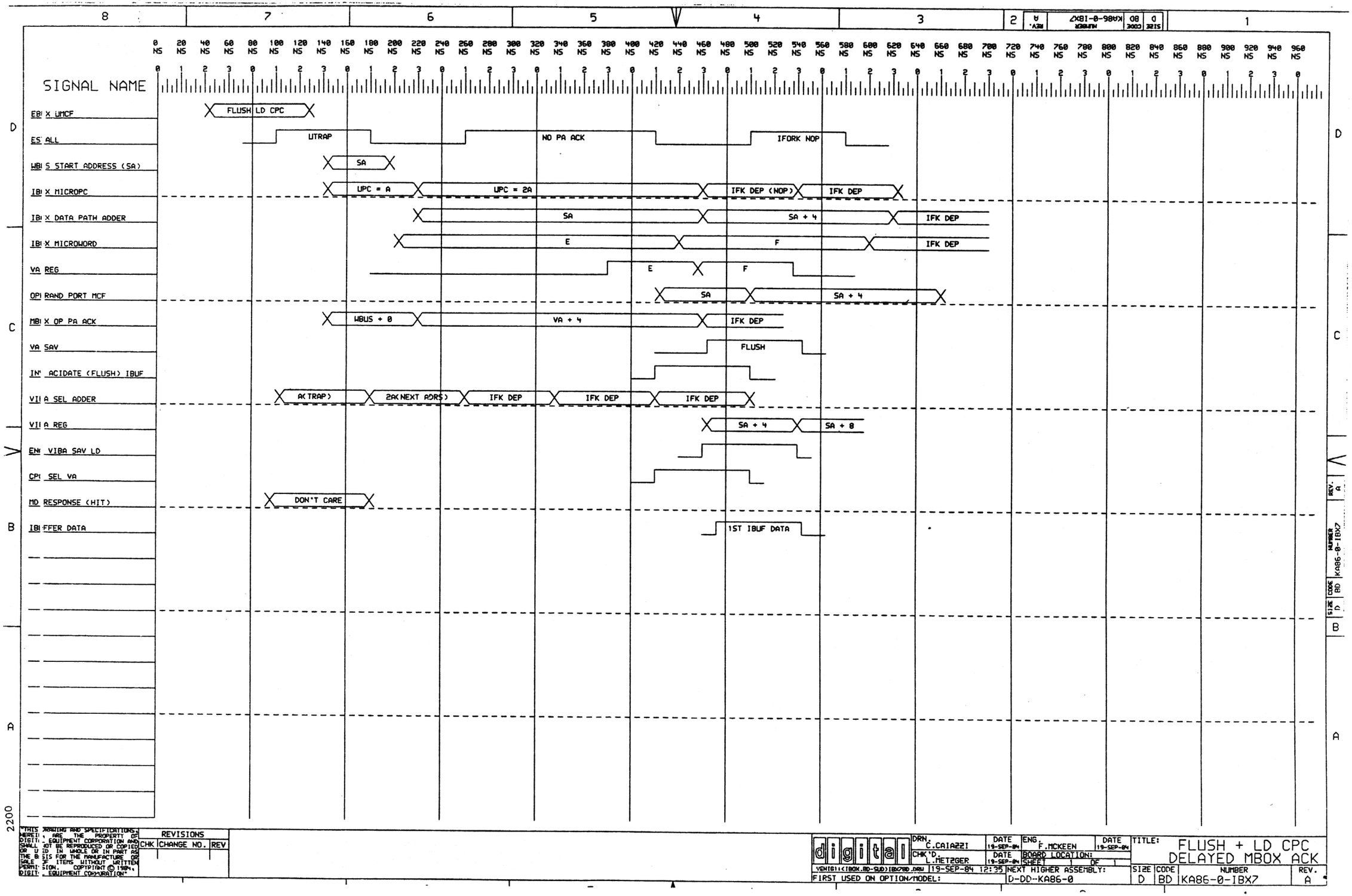
2198

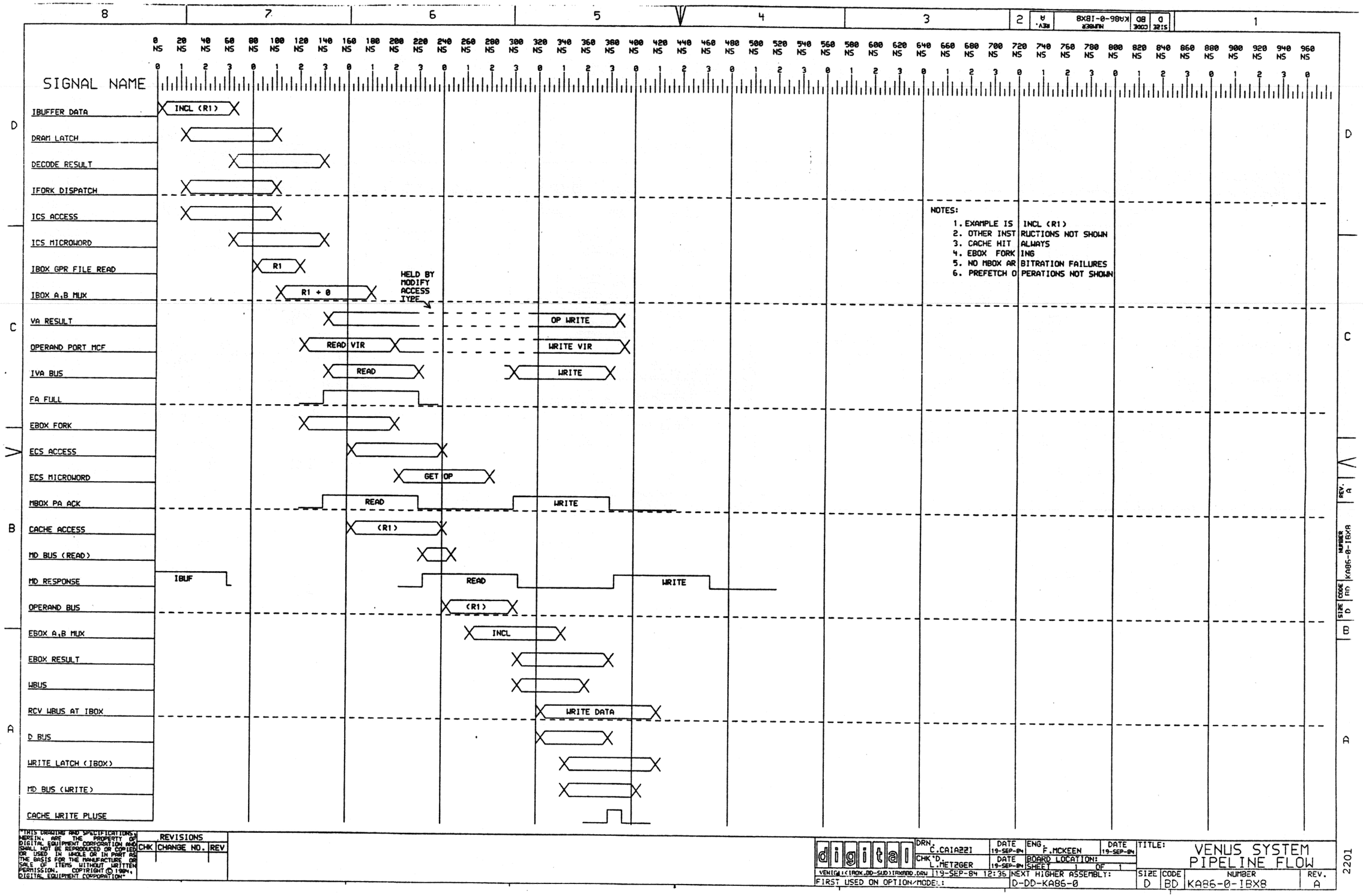


REVISIONS		
CHK	CHANGE NO.	REV

DRN. B.CHARBONNEAU	DATE 19-SEP-84	ENG. F.MCKEEN	DATE 19-SEP-84	TITLE: VIBA SEL ADDER INV IBUF	
CHK'D. L.METZGER	DATE 19-SEP-84	BOARD LOCATION: SHEET 1 OF 1			
VERIFICATION PROGRAM: 19-SEP-84 12:35		NEXT HIGHER ASSEMBLY:		SIZE D / CODE BD / NUMBER KA86-0-IBX6	REV. A
IF FIRST USED ON OPTION/MODEL:		D-DD-KA86-0			

2199


SIGNAL NAME
EBI X UMCF
ES ALL
WBI S START ADDRESS (SA)
IBI X MICROPC
IBI X DATA PATH ADDER
IBI X MICROWORD
VA REG
OPI RAND PORT MCF
MBI X OP PA ACK
VA SAV
IN ACIDATE (FLUSH) IBUF
VII A SEL ADDER
VII A REG
EN VIBA SAV LD
CPI SEL VA
MD RESPONSE (HIT)
IBI FFER DATA
FLUSH LD CPC
UTRAP
NO PA ACK
IFORK NOP
SA
UPC = A
UPC = 2A
IFK DEP (NOP)
IFK DEP
SA
SA + 4
IFK DEP
E
F
IFK DEP
E
F
SA
SA + 4
WBUS + 0
VA + 4
IFK DEP
FLUSH
A(TRAP)
2A(NEXT ADRS)
IFK DEP
IFK DEP
IFK DEP
SA + 4
SA + 8
DON'T CARE
1ST IBUF DATA
REVISIONS
CHK
CHANGE NO.
REV
DRN C.CAIA22I
CHK'D L.METZGER
ENG F.MCKEEN
BOARD LOCATION:
SHEET 1 OF 1
TITLE: FLUSH + LD CPC DELAYED MBOX ACK
NEXT HIGHER ASSEMBLY:
D-DD-KA86-0
SIZE D
CODE BD
NUMBER KA86-0-IBX7
REV. A


SIGNAL NAME
IBUFFER DATA
DRAM LATCH
DECODE RESULT
IFORK DISPATCH
ICS ACCESS
ICS MICROWORD
IBOX GPR FILE READ
IBOX A,B MUX
VA RESULT
OPERAND PORT MCF
IVA BUS
FA FULL
EBOX FORK
ECS ACCESS
ECS MICROWORD
MBOX PA ACK
CACHE ACCESS
MD BUS (READ)
MD RESPONSE
OPERAND BUS
EBOX A,B MUX
EBOX RESULT
WBUS
RCV WBUS AT IBOX
D BUS
WRITE LATCH (IBOX)
MD BUS (WRITE)
CACHE WRITE PLUSE
INCL (R1)
R1
R1 + 0
HELD BY MODIFY ACCESS TYPE
OP WRITE
READ VIR
WRITE VIR
READ
WRITE
GET OP
READ
WRITE
(R1)
IBUF
READ
WRITE
(R1)
INCL
WRITE DATA
NOTES:
1. EXAMPLE IS INCL (R1)
2. OTHER INSTRUCTIONS NOT SHOWN
3. CACHE HIT ALWAYS
4. EBOX FORKING
5. NO MBOX ARBITRATION FAILURES
6. PREFETCH OPERATIONS NOT SHOWN
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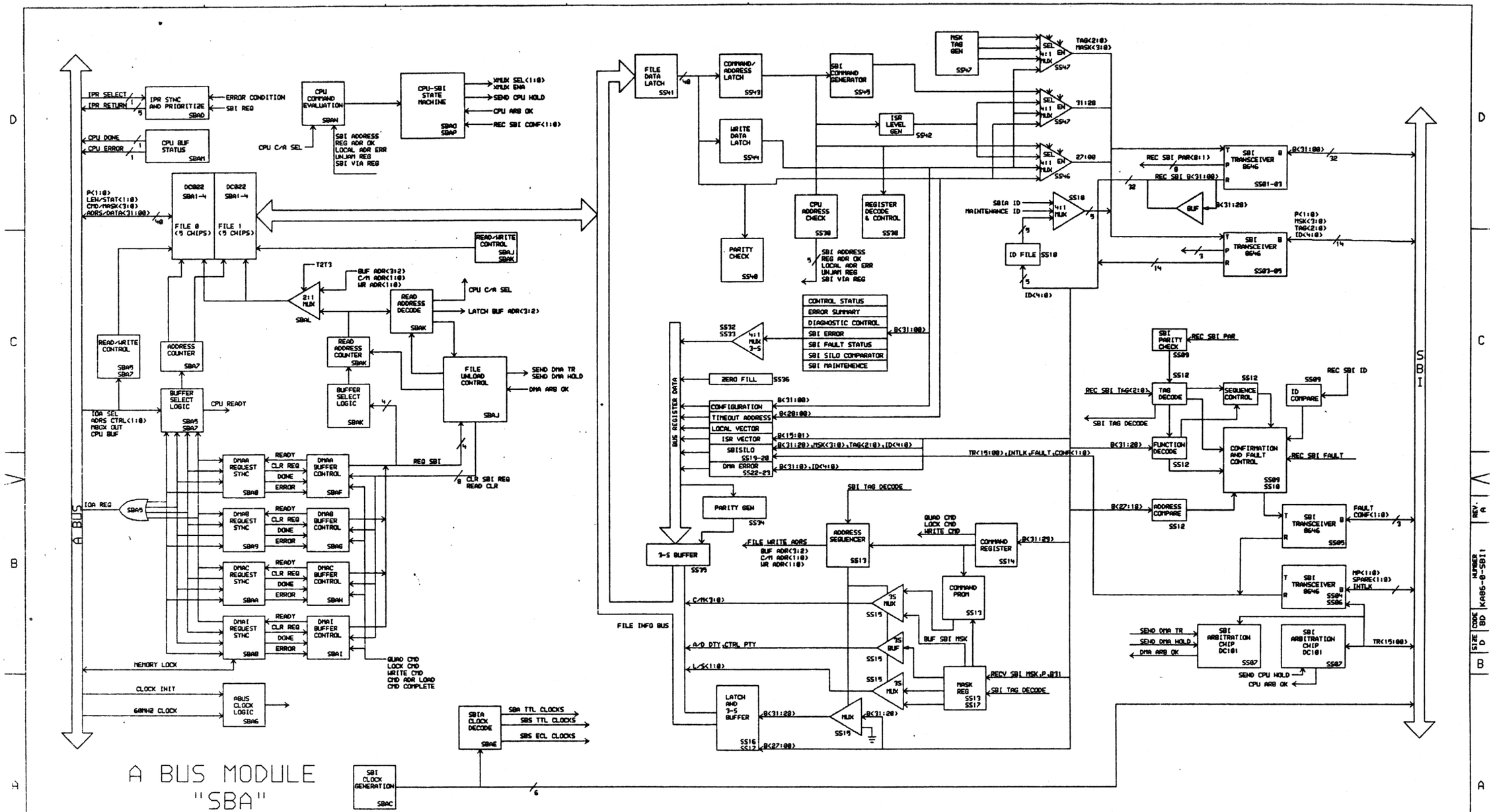
REVISIONS
CHK | CHANGE NO. | REV
digital
DRN. C.CAIAZZI DATE 19-SEP-84
CHK'D. L.METZGER DATE 19-SEP-84
ENG. F.MCKEEN DATE 19-SEP-84
BOARD LOCATION:
SHEET 1 OF 1
TITLE: VENUS SYSTEM PIPELINE FLOW
VENUS:[IBOX.DD-SUD]IBXMAP.DAV 19-SEP-84 12:36
FIRST USED ON OPTION/MODE:
NEXT HIGHER ASSEMBLY: D-DD-KA86-0
SIZE D | CODE BD | NUMBER KA86-0-IBX8 | REV. A
REV. A
SIZE D | CODE BD | NUMBER KA86-0-IBXA
2201



REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. L.Toomey 18-SEP-84 | ENG. J.MARTIN 18-SEP-84 | TITLE: SBIA BLOCK DIAGRAM

CHK'D. L.METZGER 18-SEP-84 | BOARD LOCATION: | SHEET 1 OF 1

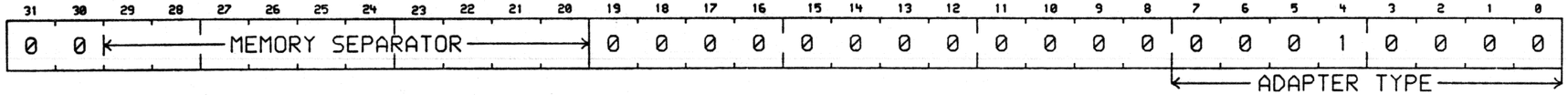
VENMG2:<MARTIN>SBI1BD.DRW 18-SEP-84 14:15 | NEXT HIGHER ASSEMBLY: D-DD-KA86-0

FIRST USED ON OPTION/MODEL:

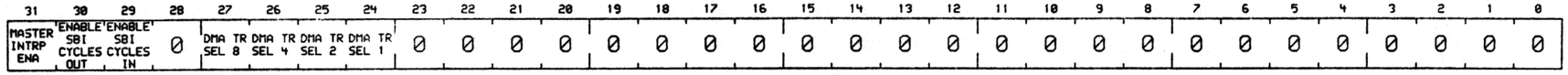
SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI1	A

2202

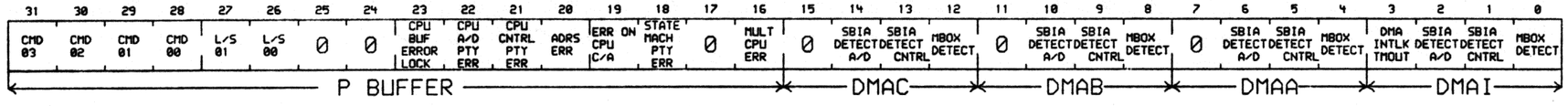
CONFIGURATION
2X08 0000



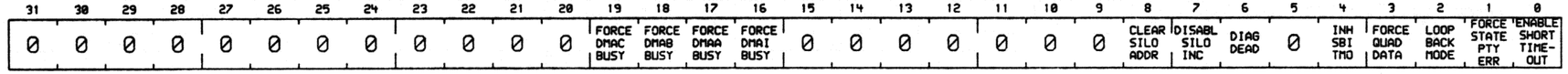
CTRL/STATUS
2X08 0004



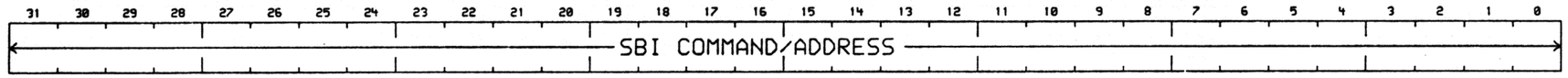
ERROR SUMMARY
2X08 0008



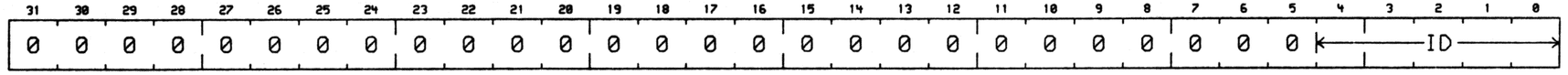
DIAGNOSTIC CONTROL
2X08 000C



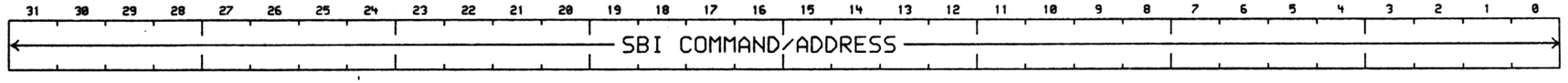
DMAI CMD/ADRS
2X08 0010



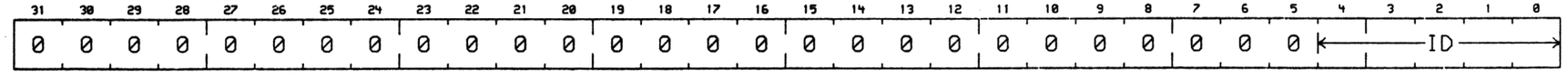
DMAI ID
2X08 0014



DMAA CMD/ADRS
2X08 0018



DMAA ID
2X08 001C



REVISIONS

CHK	CHANGE NO.	REV

digital

DRN. D.Toomey DATE 18-SEP-84
CHK D. L.METZGER DATE 18-SEP-84
ENG. J.MARTIN DATE 18-SEP-84
BOARD LOCATION:
SHEET 1 OF 1

VENMG2:<MARTIN>SBI2BD.DAW 17-SEP-84 14:54
FIRST USED ON OPTION/MODEL:
NEXT HIGHER ASSEMBLY: D-DD-KA86-0

TITLE: SBIA REGISTERS PART1

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI2	A

2203

DMAB CMD/ADDRS
2X08 0020

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBI COMMAND/ADDRESS																															

DMAB ID
2X08 0024

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ID				

DMAC CMD/ADDRS
2X08 0028

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SBI COMMAND/ADRESS																															

DMAC ID
2X08 002C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ID				

SBI SILO
2X08 0030

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AFTER FAULT	0	SBI ID4	SBI ID3	SBI ID2	SBI ID1	SBI ID0	SBI TAG2	SBI TAG1	SBI TAG0	SBI M3 OR B31	SBI M2 OR B30	SBI M1 OR B29	SBI M0 OR B28	SBI CNF1	SBI CNF0	SBI TR15	SBI TR14	SBI TR13	SBI TR12	SBI TR11	SBI TR10	SBI TR09	SBI TR08	SBI TR07	SBI TR06	SBI TR05	SBI TR04	SBI TR03	SBI TR02	SBI TR01	SBI TR00

SBI ERROR
2X08 0034

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CP TMOUT	CP TMOUT STAT1	CP TMOUT STAT0	0	CP SBI ERROR CONF	0	0	0	0	0	0	0	0

SBI
TIMEOUT ADDRESS
2X08 0038

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	PHYS ADDR 27	PHYS ADDR 26	PHYS ADDR 25	PHYS ADDR 24	PHYS ADDR 23	PHYS ADDR 22	PHYS ADDR 21	PHYS ADDR 20	PHYS ADDR 19	PHYS ADDR 18	PHYS ADDR 17	PHYS ADDR 16	PHYS ADDR 15	PHYS ADDR 14	PHYS ADDR 13	PHYS ADDR 12	PHYS ADDR 11	PHYS ADDR 10	PHYS ADDR 09	PHYS ADDR 08	PHYS ADDR 07	PHYS ADDR 06	PHYS ADDR 05	PHYS ADDR 04	PHYS ADDR 03	PHYS ADDR 02	PHYS ADDR 01	PHYS ADDR 00

SBI
FAULT/STATUS
2X08 003C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PARITY FAULT	WR SEQ FAULT	UNEXP RD DAT FAULT	INTLK SEQ FAULT	MULTI XMIT FAULT	XMITR DURING FAULT	0	0	PI PTY ERR	PB PTY ERR	0	0	FAULT LATCH	FAULT INTRP ENA	SBI FAULT SIGNAL	FAULT SILO LOCK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

REVISIONS

CHK	CHANGE NO.	REV

digital

VENMG2:<MARTIN>SBI30D.DRW 17-SEP-84 14:55

DRN. S. Conroy DATE 10-SEP-84
CHK'D L.METZGER DATE 10-SEP-84
ENG. J.MARTIN DATE 10-SEP-84
BOARD LOCATION:
SHEET 1 OF 1
FIRST USED ON OPTION/MODEL:
NEXT HIGHER ASSEMBLY: D-DD-KA86-0

TITLE: SBIA REGISTERS PART2

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI3	A

SIZE D | CODE BD | NUMBER KA86-0-SBI3 | REV. A

2204

SBI SILO COMPARATOR 2X08 0040

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
COMP SILO LOCK	SILO LCK INT ENA	LOCK UNCND	COND LOCK CODE 01	COND LOCK CODE 00	COMP CMDMSK 03	COMP CMDMSK 02	COMP CMDMSK 01	COMP CMDMSK 00	COMP TAG 02	COMP TAG 01	COMP TAG 00	COUNT FIELD 03	COUNT FIELD 02	COUNT FIELD 01	COUNT FIELD 00	MAINT TR 15	MAINT TR 14	MAINT TR 13	MAINT TR 12	MAINT TR 11	MAINT TR 10	MAINT TR 09	MAINT TR 08	MAINT TR 07	MAINT TR 06	MAINT TR 05	MAINT TR 04	MAINT TR 03	MAINT TR 02	MAINT TR 01	MAINT TR 00

FORCE SBI REQUEST SBI MAINT. BIT 04 = 1

MAINT REQ 07	MAINT REQ 06	MAINT REQ 05	MAINT REQ 04	MAINT ALERT

SBI MAINTENANCE 2X08 0044

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FORCE P0 REV ON SBI	FORCE WSQ FAULT	*FORCE UNXPD RD DAT FAULT	*FORCE MULTI XMITTR FAULT	MAINT ID04	MAINT ID03	MAINT ID02	MAINT ID01	MAINT ID00	0	0	0	0	0	0	0	0	0	0	0	FORCE P1 REV ON SBI	0	0	FORCE TIMOUT	0	0	0	FORCE SBI REQ	FORCE MAINT TR SEQ	FORCE MAINT TR	FORCE ISR DATA	USE MAINT ID

SBI UNJAM 2X08 0048

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SBI QUADCLEAR 2X08 004C

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	1	1	0	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

VECTOR 2X08 0080 TO 2X08 00B8

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X	X	X	X	X	X

REVISIONS

CHK	CHANGE NO.	REV

digital

DRN. J. Timothy — DATE 18-SEP-84 — ENG. J.MARTIN — DATE 18-SEP-84

CHK D. L. METZGER — DATE 18-SEP-84 — BOARD LOCATION: — SHEET 1 OF 1

VENMG2::<MARTIN>SBI14BD.DRW 17-SEP-84 14:56 — NEXT HIGHER ASSEMBLY: D-DD-KA86-0

FIRST USED ON OPTION/MODEL:

TITLE: SBIA REGISTERS PART 3

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI4	A

2205

FUNCTION (INFORMATION TO BE TRANSMITTED ON THE SBI)	SPECIAL CASES	MASK, TAG MUX SEL A1 A0	B<31:28> MUX SEL A1 A0	B<27:00> MUX SEL A1 A0	TAG SOURCE	MASK SOURCE	B<31:28> SOURCE	B<27:00> SOURCE	PREDICT P1 SOURCE	PREDICT P0 SOURCE	COMMENTS
DMA READ DATA RETURN	NO ERROR	0 0	0 0	0 0	FORCED (000)	FORCED (0000)	FILE DATA LATCH	FILE DATA LATCH	-LATCH A/D PAR	0(-ERROR)	
	PARITY ERROR OR L/S NOT 00	0 0	0 0	0 0	FORCED (000)	FORCED (0010)	FILE DATA LATCH	FILE DATA LATCH	LATCH A/D PAR	1(ERROR)	
CPU CMD/ADR											
READ		0 1	0 1	0 1	FORCED (011)	CPU ADRS LATCH L/S	SBI FUNCTION GEN	CPU ADRS LATCH	CPU ADRS PAR	FORCED (0)	
WRITE		0 1	0 1	0 1	FORCED (011)	WRITE DATA LATCH MASK	SBI FUNCTION GEN	CPU ADRS LATCH	CPU ADRS PAR	-DATA CNTRL PAR (WRITE DATA LATCH)	
QUADCLEAR		1 0	1 0	1 0	FORCED (011)	WRITE DATA LATCH MASK	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	-DATA CNTRL PAR (WRITE DATA LATCH)	
CPU WRITE DATA											
WRITE COMMAND	NORMAL	1 0	1 0	1 0	FORCED (101)	FORCED (0000)	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	FORCED (0)	
	FORCE WRITE SEQ FAULT	1 0	1 0	1 0	FORCED (111)	FORCED (0000)	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	FORCED (1)	DIAGNOSTIC MODE
QUADCLEAR WD1	NORMAL	1 0	1 0	1 0	FORCED (101)	WRITE DATA LATCH MASK	DISABLED (0)	DISABLED (0)	DISABLED (0)	-DATA CNTRL PAR (WRITE DATA LATCH)	
	FORCE WRITE SEQ FAULT	1 0	1 0	1 0	FORCED (111)	WRITE DATA LATCH MASK	DISABLED (0)	DISABLED (0)	DISABLED (0)	-DATA CNTRL PAR (WRITE DATA LATCH)	DIAGNOSTIC MODE
	FORCE QUAD DATA	1 0	1 0	1 0	FORCED (101)	WRITE DATA LATCH MASK	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	-DATA CNTRL PAR (WRITE DATA LATCH)	DIAGNOSTIC MODE
QUADCLEAR WD2	NORMAL	1 0	1 0	1 0	FORCED (101)	FORCED (0000)	DISABLED (0)	DISABLED (0)	DISABLED (0)	FORCED (0)	
	FORCE WRITE SEQ FAULT	1 0	1 0	1 0	FORCED (111)	FORCED (0000)	DISABLED (0)	DISABLED (0)	DISABLED (0)	FORCED (1)	DIAGNOSTIC MODE
	FORCE QUAD DATA	1 0	1 0	1 0	FORCED (101)	FORCED (0000)	WRITE DATA LATCH	WRITE DATA LATCH	-CPU DATA PAR (WRITE DATA LATCH)	FORCED (0)	DIAGNOSTIC MODE
INTERRUPT SUMMARY READ		1 1	1 1	1 1	FORCED (110)	FORCED (0000)	FORCED (0000)	<27:08> FORCED (0) <07:04>DECODE OF CPU ADR<01:00> <03:00>FORCED (0)	FORCED (1)	FORCED (0)	
ISR RESPONCE	NORMAL	-----	-----	-----	-----	-----	-----	-----	-----	-----	NO TRANSMIT
	FORCE ISR DATA	1 0	1 0	1 0	DISABLED (0)	FORCED (0000)	WRITE DATA LATCH	WRITE DATA LATCH	FORCED (0)	FORCED (0)	

S-DATA ASSEMBLY DATA PATH MUXING

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. | DATE 18-SEP-84 | ENG. J.MARTIN | DATE 18-SEP-84
CHK'D L.METZGER | DATE 18-SEP-84 | BOARD LOCATION: | SHEET 1 OF 1

VENMG2:<MARTIN>SB1580.DRW 18-SEP-84 10:46 | NEXT HIGHER ASSEMBLY: D-DD-KA86-0

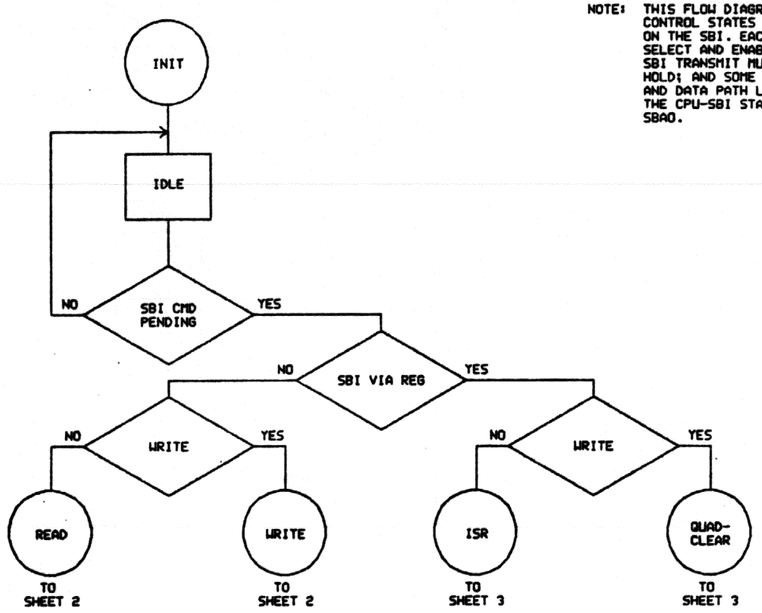
FIRST USED ON OPTION/MODEL:

TITLE: S-DATA PATH OUTPUT MUXING

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SB15	A

2206

NOTE: THIS FLOW DIAGRAM DESCRIBES THE CONTROL STATES FOR CPU TRANSACTIONS ON THE SBI. EACH STATE HAS SPECIFIC SELECT AND ENABLE INFORMATION FOR THE SBI TRANSMIT MUX; FOR SENDING SBI HOLD; AND SOME STATES TRIGGER CONTROL AND DATA PATH LOGIC.
THE CPU-SBI STATE LOGIC IS ON SHEET SBA0.



CPU-SBI STATE MACHINE FLOW DIAGRAM

REVISIONS		
CHK	CHANGE NO.	REV

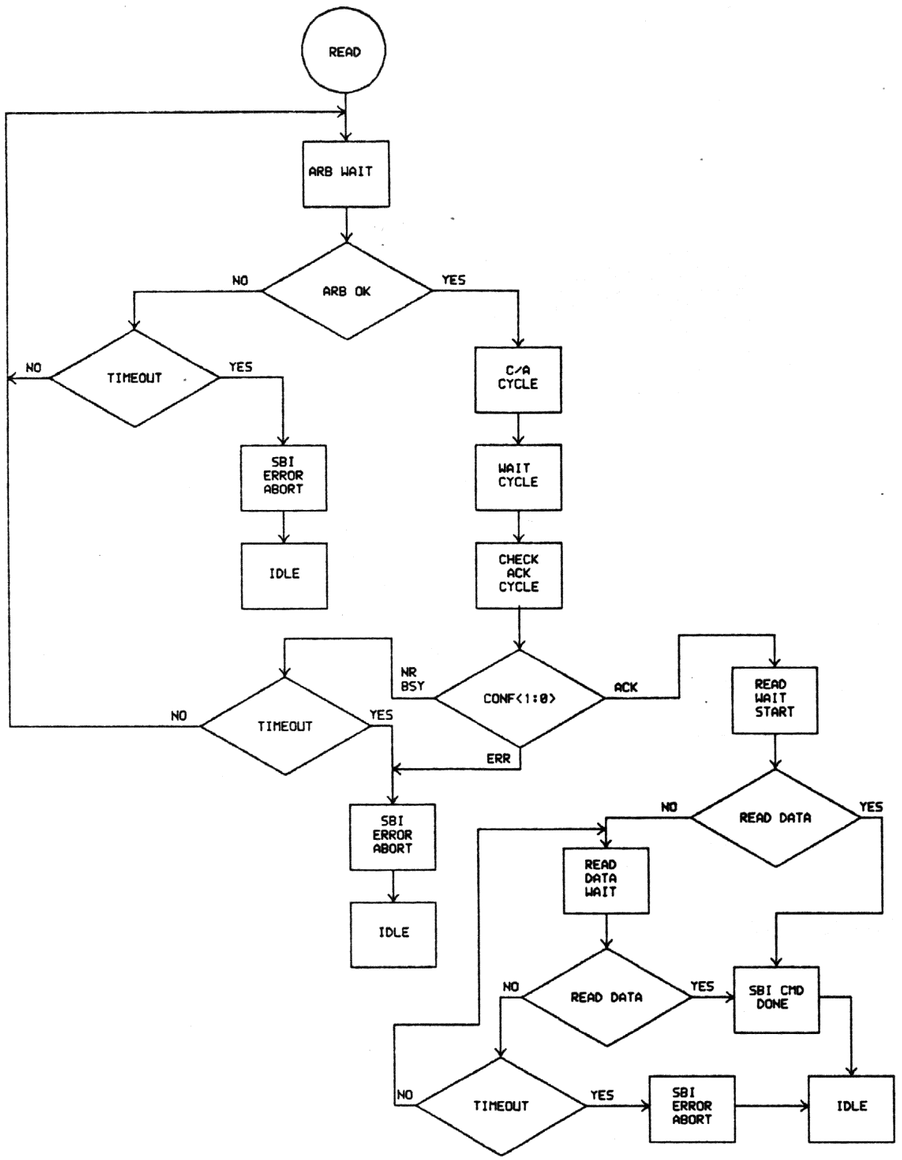
digital

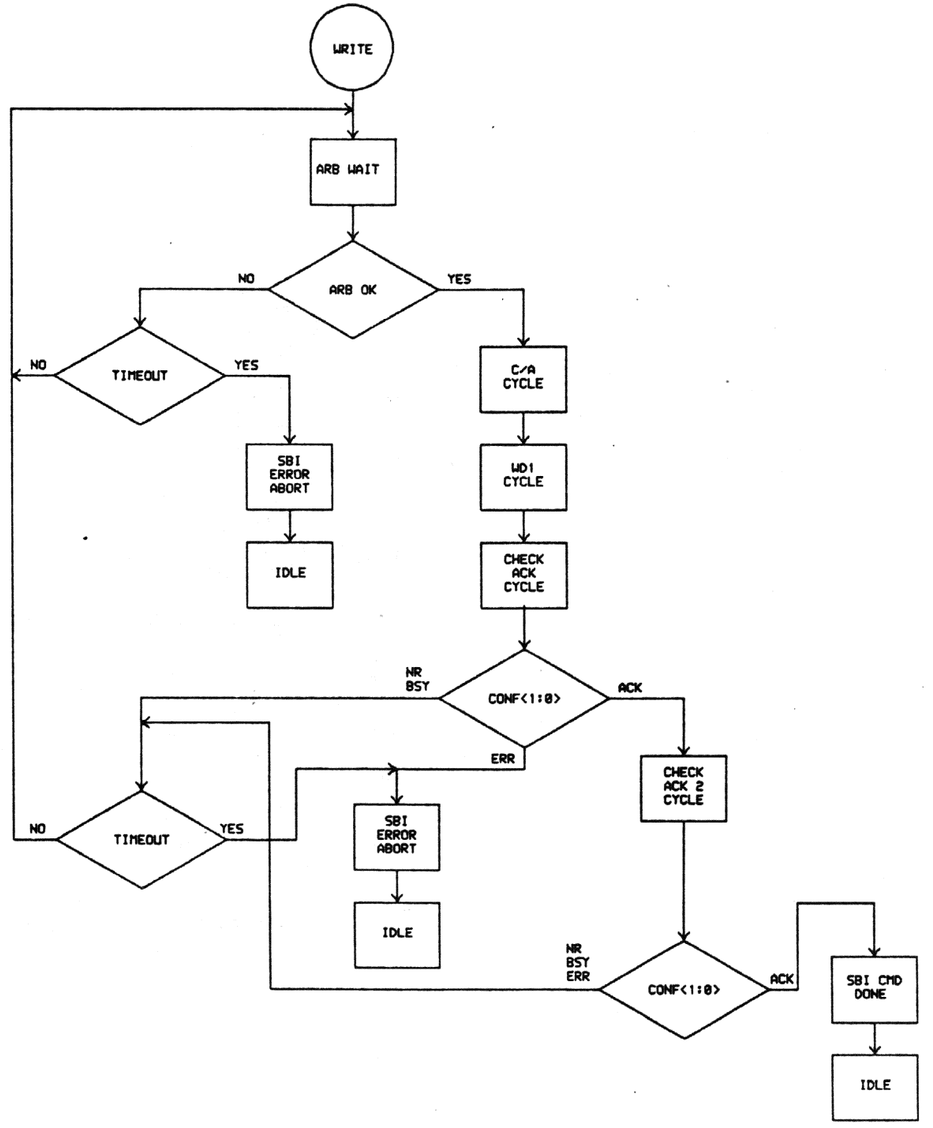
DRN. L.Toomby 18-SEP-84 | ENG. J.MARTIN 18-SEP-84
CHK'D. L.METZGER 18-SEP-84 | BOARD LOCATION: SHEET 1 OF 1
VENNG2::<MARTIN>SBIG80.DRV 18-SEP-84 10:48 | NEXT HIGHER ASSEMBLY: D-DD-KA86-0
FIRST USED ON OPTION/MODEL:

TITLE: CPU-SBI STATE MACHINE FLOW

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI6	A

2207





CPU-SBI STATE MACHINE FLOW DIAGRAM

REVISIONS		
CHK	CHANGE NO.	REV

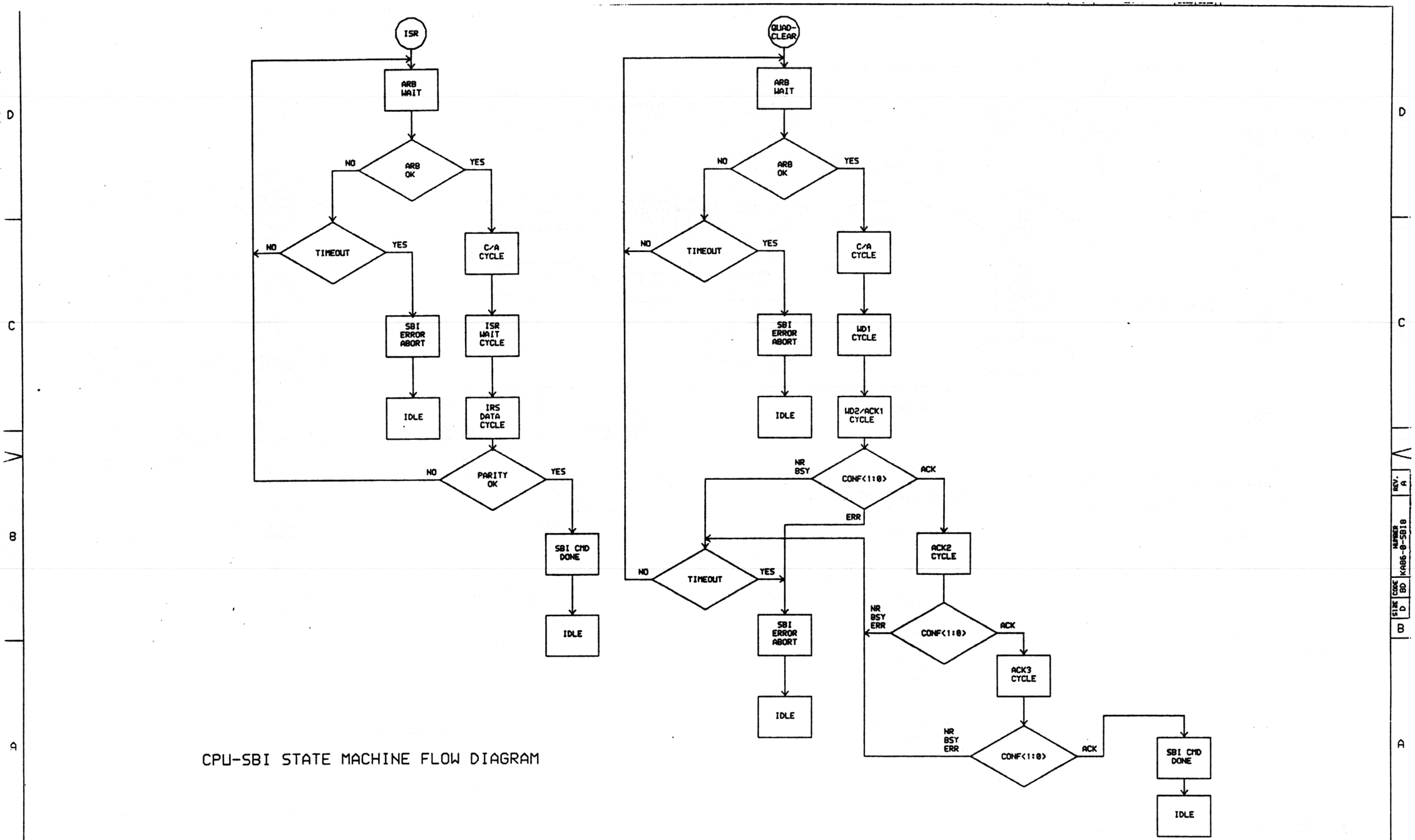
digital

DRN. D. Landy
CHK D. L.METZGER
DATE 18-SEP-84
ENG. J.MARTIN
DATE 18-SEP-84
DATE 18-SEP-84
BOARD LOCATION:
SHEET 1 OF 1
VENMG2:<MARTIN>SBI780.DRW 18-SEP-84 10:54
NEXT HIGHER ASSEMBLY: D-DD-KA86-0
FIRST USED ON OPTION/MODEL:

TITLE: SBI STATE MACHINE READ/WRITE

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI7	A

2208



CPU-SBI STATE MACHINE FLOW DIAGRAM

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. L.Toomey 18-SEP-84 | ENG. J.MARTIN 18-SEP-84 | TITLE: SBI STATE MACHINE ISR/QUADCLEAR

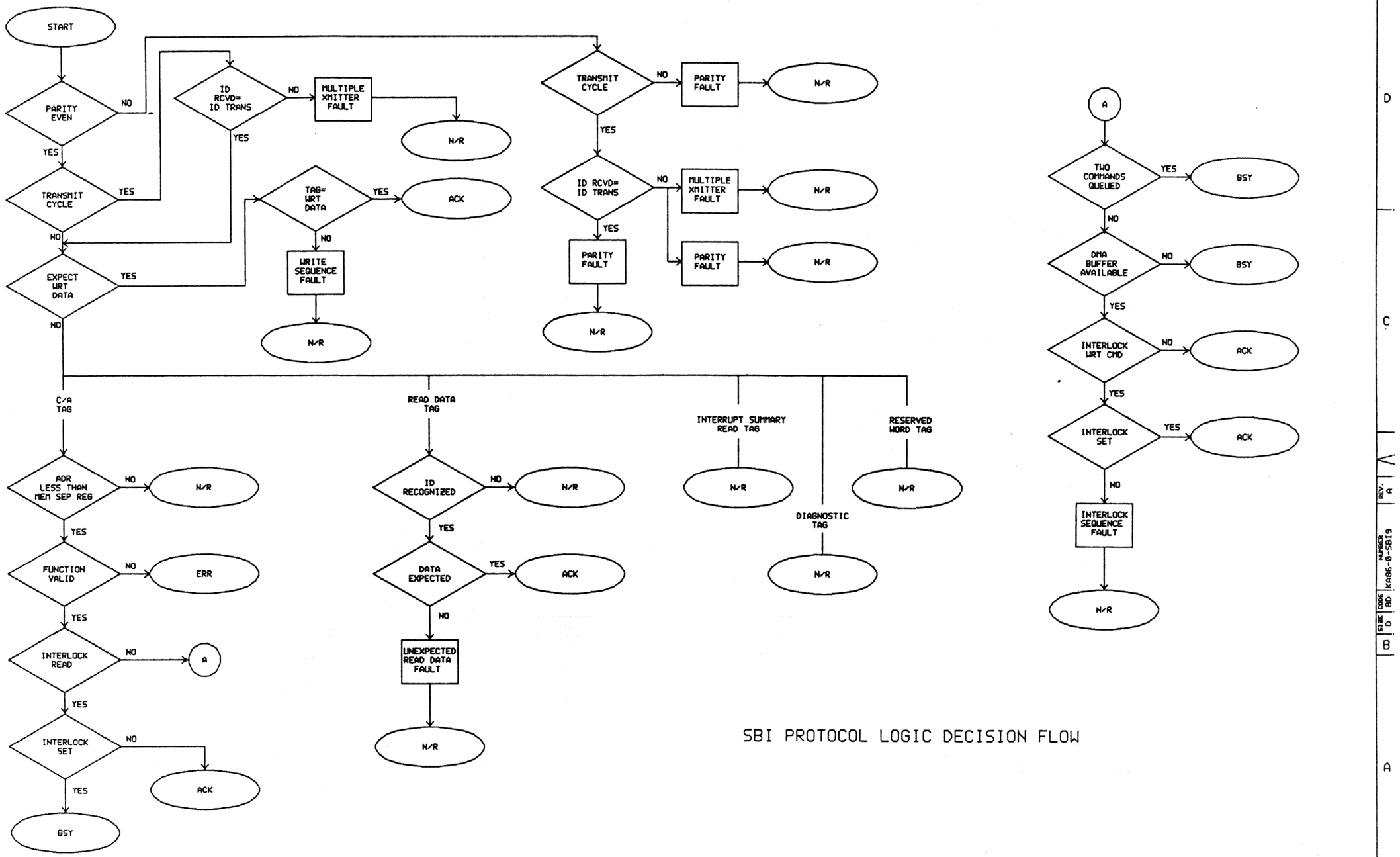
CHK D. L.METZGER 18-SEP-84 | BOARD LOCATION: | SHEET 1 OF 1

VENHG2:<MARTIN>SBI88D.DRW 18-SEP-84 10:57 | NEXT HIGHER ASSEMBLY: D-DD-KA86-0

FIRST USED ON OPTION/MODEL:

SIZE	CODE	NUMBER	REV.
D	BD	KA86-0-SBI8	A

2209

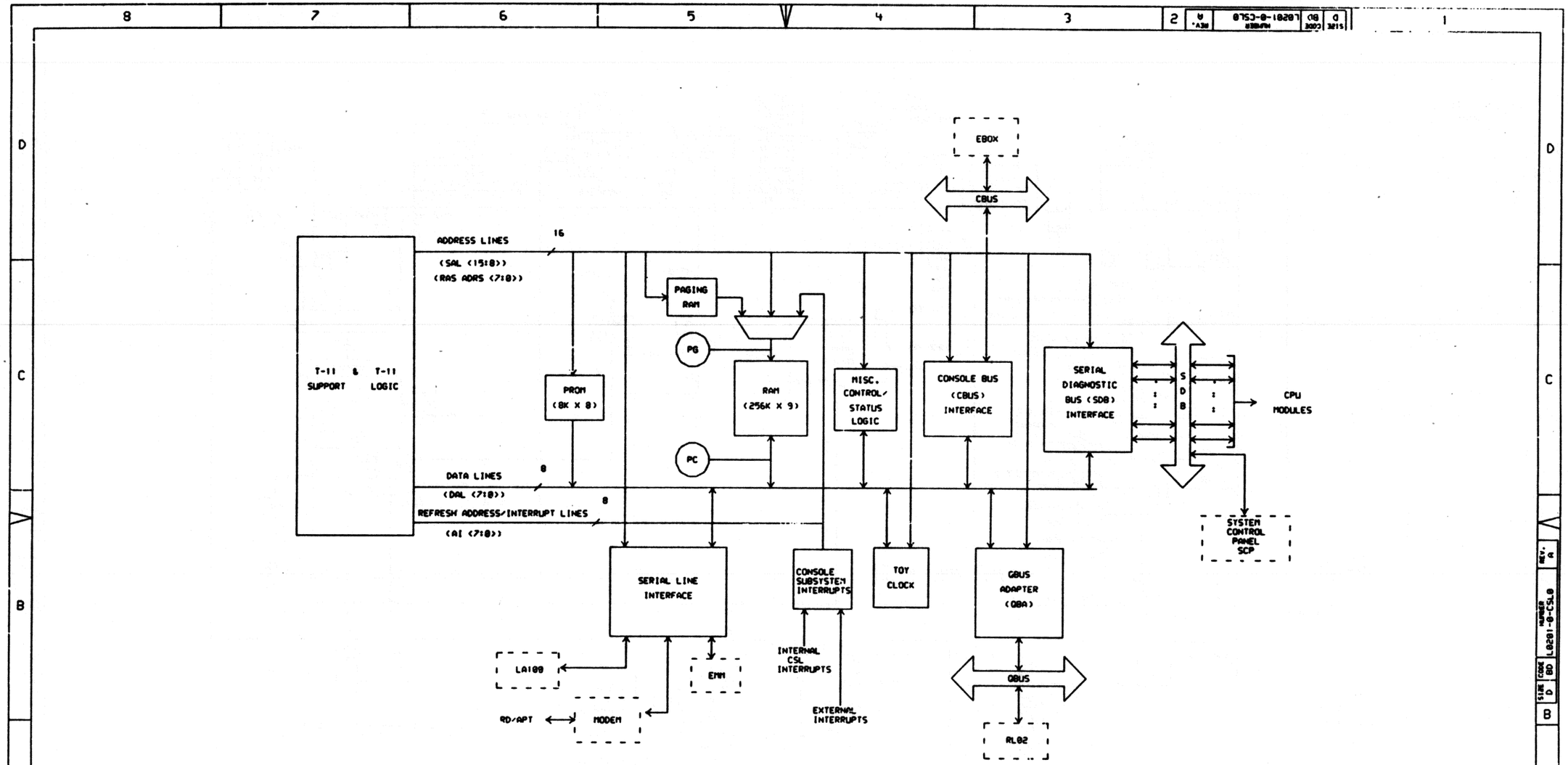


SBI PROTOCOL LOGIC DECISION FLOW

REVISIONS		
CHK	CHANGE NO.	REV

DRN. L.Toomsky	DATE 18-SEP-84	ENG. J.MARTIN	DATE 18-SEP-84	TITLE: SBI PROTOCOL DECISION FLOW	
CHK D. L.METZGER	DATE 18-SEP-84	BOARD LOCATION: SHEET 1 OF 1			
VENMG2::<MARTIN>SBI98D.DRW 18-SEP-84 10:58		NEXT HIGHER ASSEMBLY: D-DD-KA86-0		SIZE D	CODE BD
FIRST USED ON OPTION/MODEL:				NUMBER KA86-0-SBI9	REV. A

2210



PG = PARITY GENERATE
PC = PARITY CHECK

FIGURE 1-1 CONSOLE (CSL) MODULE

REVISIONS

CHK	CHANGE NO.	REV

digital

DRN. R.DAME — DATE 01-NOV-84
CHK'D L.METZGER — DATE 01-NOV-84
ENG. E.ANTON — DATE 01-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:(COM2)CSL0BD.DRW 19-OCT-84 11:36
NEXT HIGHER ASSEMBLY: D-DD-L0201-0
FIRST USED ON OPTION/MODEL:

TITLE: CONSOLE (CSL) MODULE

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL0	.)

REV. A

2211

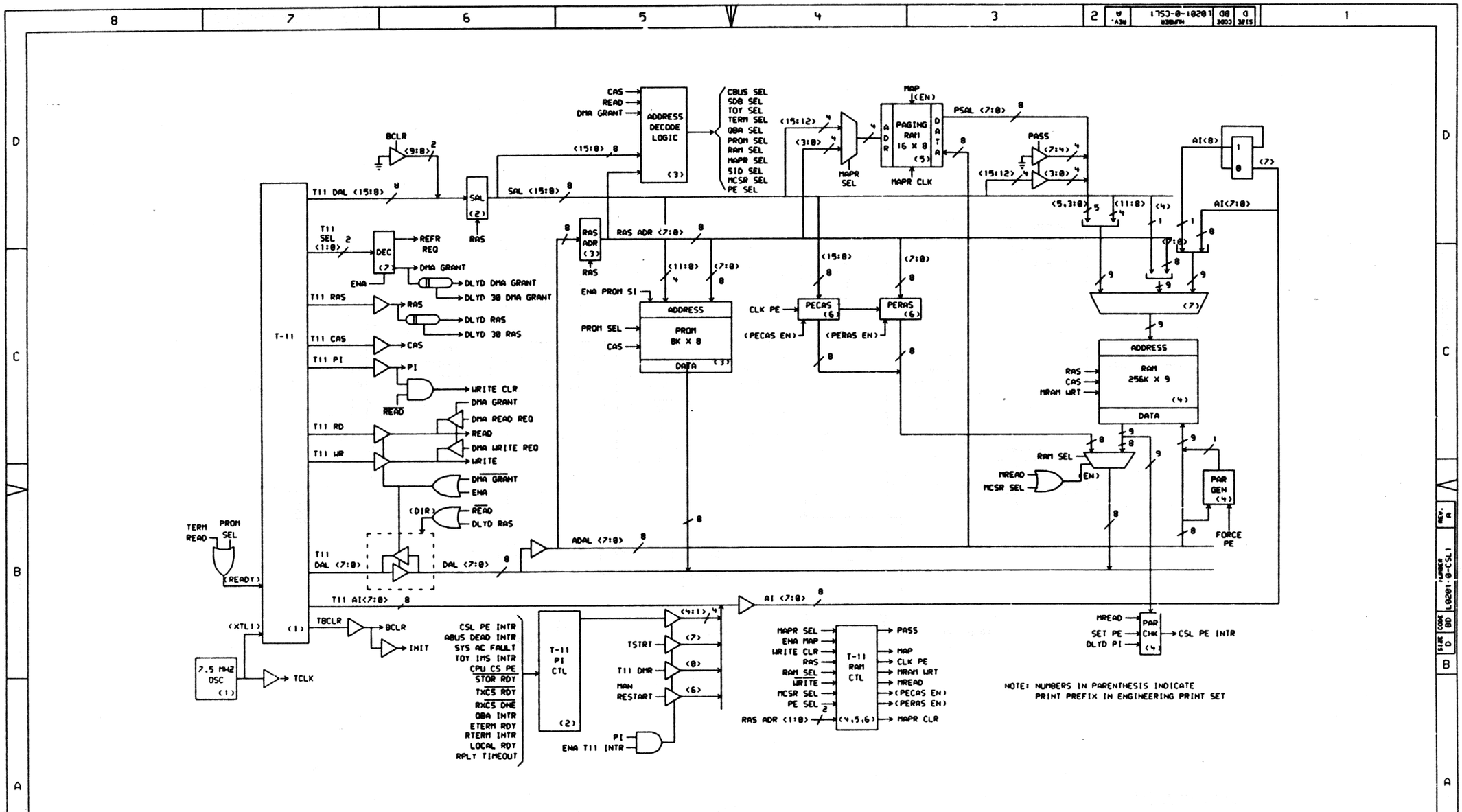


FIGURE 2-1 T-11 MICROPROCESSOR PLUS MEMORY AND SUPPORT LOGIC

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. R.DAME | DATE 01-NOV-84 | ENG. E.ANTON | DATE 01-NOV-84

CHK'D L.METZGER | DATE 01-NOV-84 | BOARD LOCATION:

ELF:<COM2>CSL1BD.DRW 23-OCT-84 10:07 | SHEET 1 OF 1 | NEXT HIGHER ASSEMBLY:

FIRST USED ON OPTION/MODEL: | D-DD-L0201-0

TITLE: T-11 MICRO MEM AND SUPRT LOGIC

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL1	A

2212

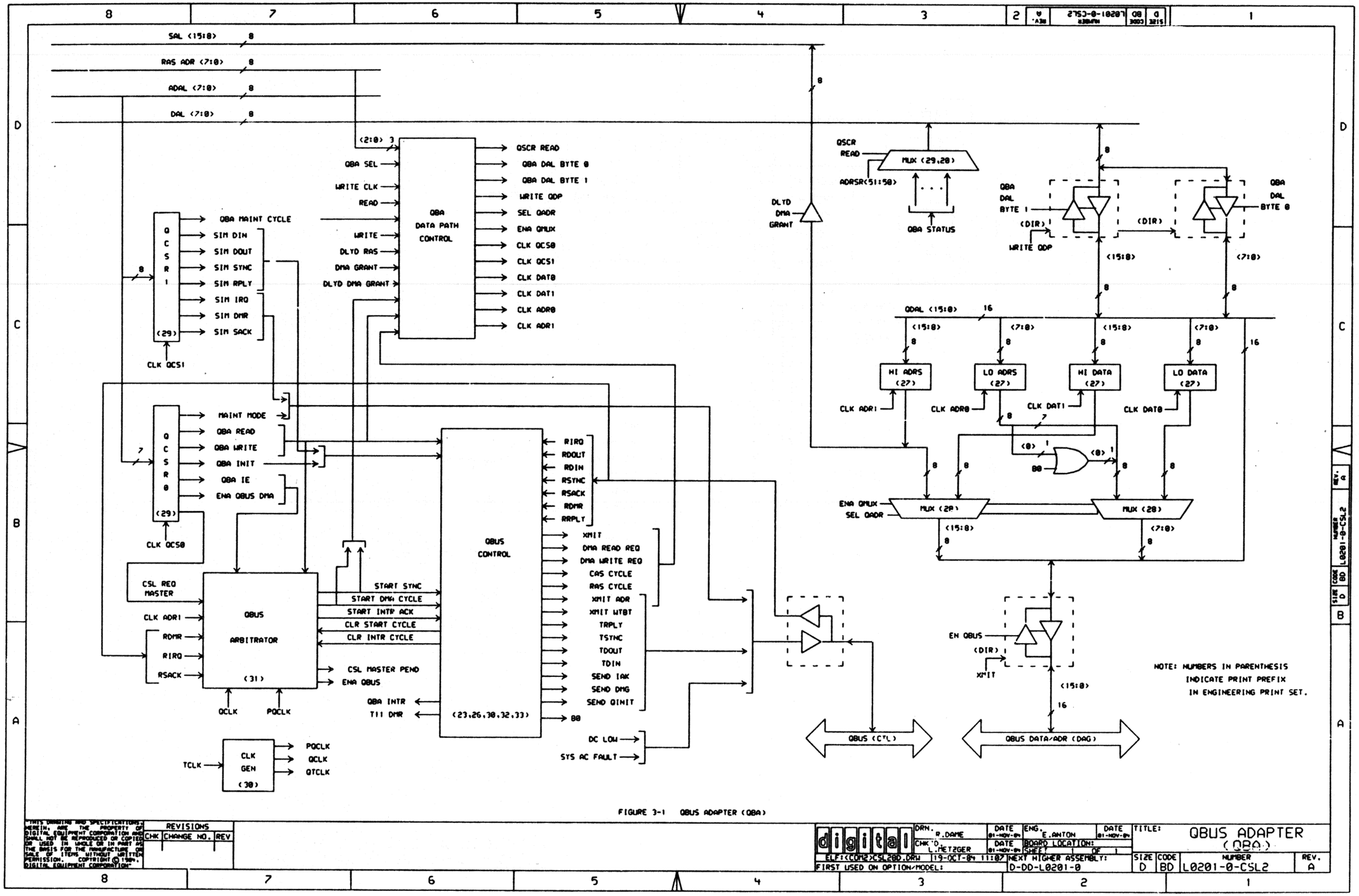


FIGURE 3-1 QBUS ADAPTER (QBA)

REVISIONS		
CHK	CHANGE NO.	REV

DRN. R.DAME	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84
CHK'D L.METZGER	DATE 01-NOV-84	BOARD LOCATION:	
ELF:<COM2>CSL2BD.DRW 19-OCT-84 11:07		SHEET 1 OF 1	
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-L0201-0	

TITLE: QBUS ADAPTER (QBA)

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL2	A

2213

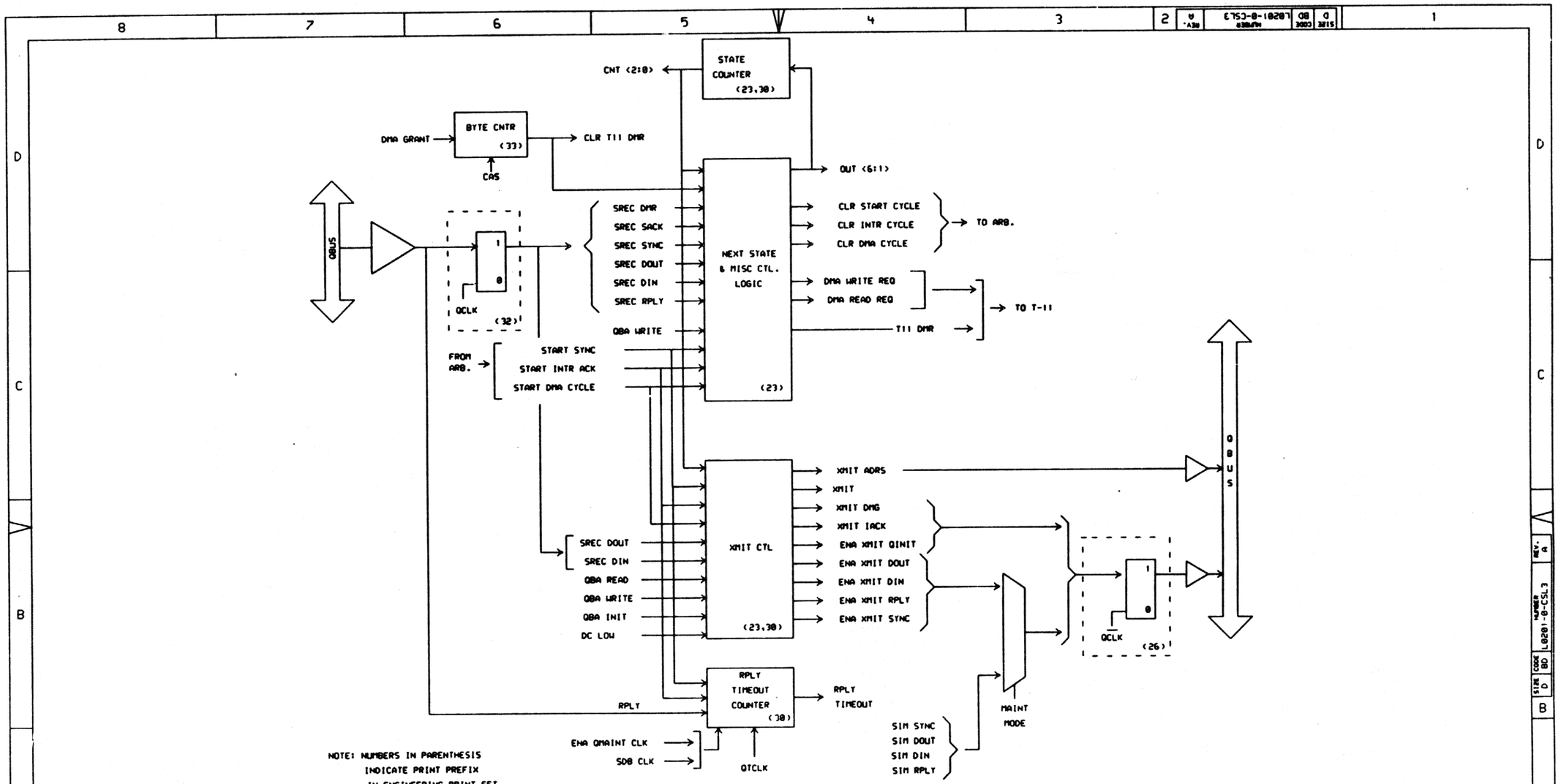


FIGURE 3-2 QBUS CONTROL

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. R.DAME — DATE 01-NOV-84
CHK'D L.METZGER — DATE 01-NOV-84
ENG. E.ANTON — DATE 01-NOV-84
BOARD LOCATION:
SHEET OF
ELF:<COM2>CSL3BD.DRW 19-OCT-84 11:07
NEXT HIGHER ASSEMBLY: D-DD-L0201-0
FIRST USED ON OPTION/MODEL:

TITLE: QBUS CONTROL

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL3	A

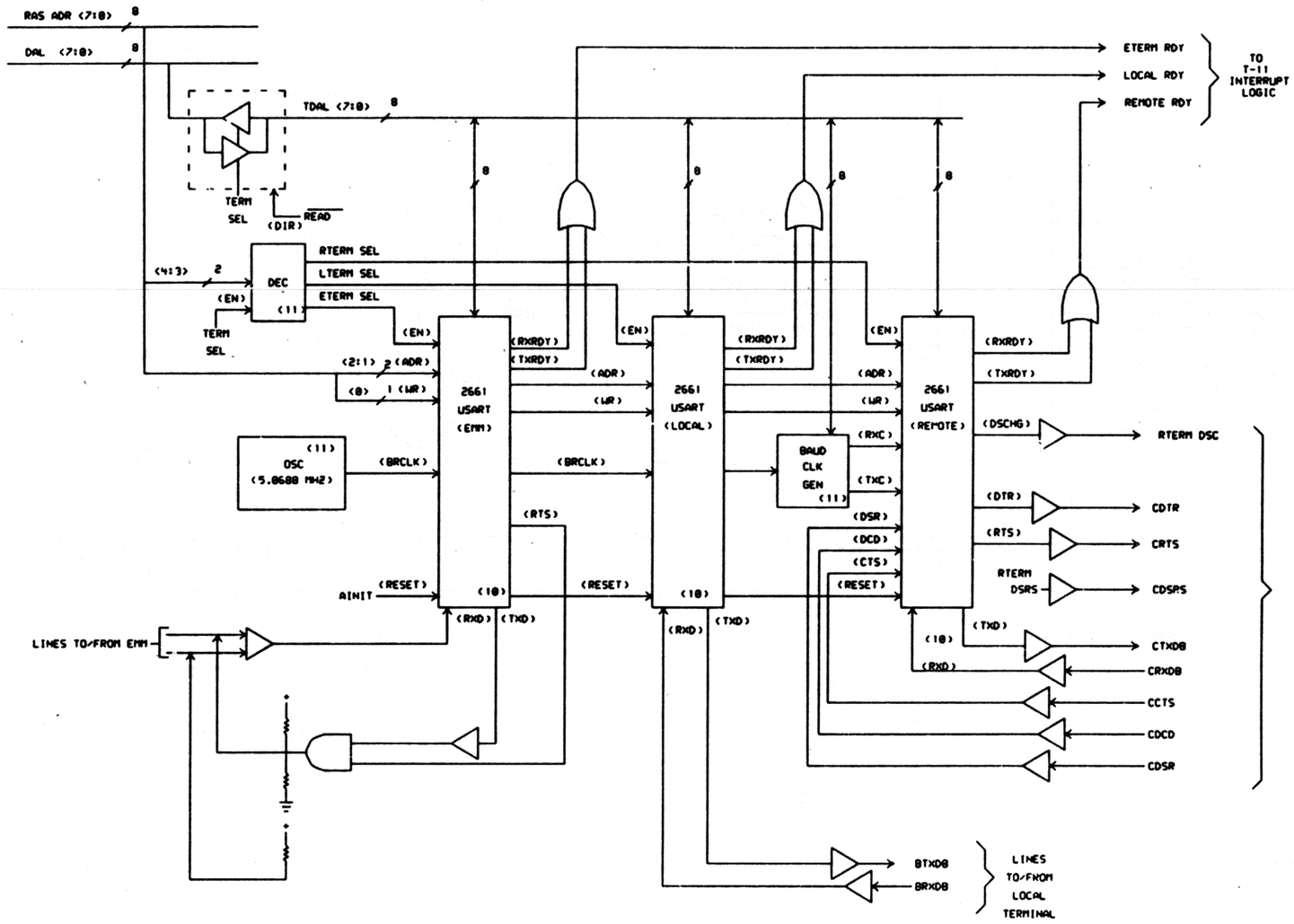


FIGURE 4-1 SERIAL DATA INTERFACE

REVISIONS		
CHK	CHANGE NO.	REV

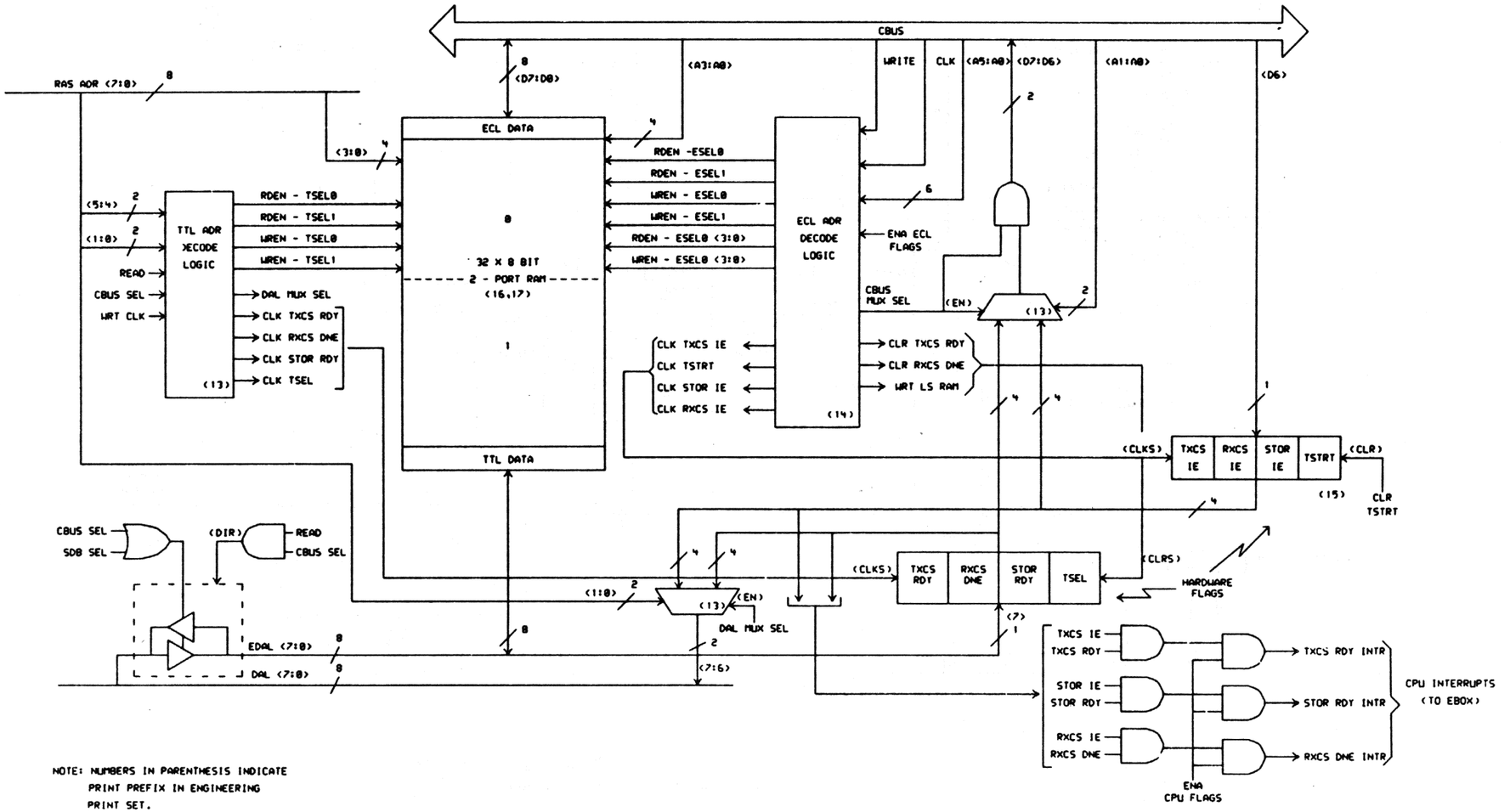
digital

DRN. R.DAME	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84
CHK'D. L.METZGER	DATE 01-NOV-84	BOARD LOCATION:	
ELF:(COM2)CSL4BD.DRW 19-OCT-84 11:00		SHEET 1 OF 1	
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-L0201-0	

TITLE: SERIAL DATA INTERFACE

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL4	A

2215



NOTE: NUMBERS IN PARENTHESIS INDICATE
PRINT PREFIX IN ENGINEERING
PRINT SET.

FIGURE 6-1 CBUS INTERFACE

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. R.DAME	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84	TITLE: CBUS INTERFACE	
CHK'D L.METZGER	DATE 01-NOV-84	BOARD LOCATION:	SHEET 1 OF 1		
ELF:<COM2>CSL5BD.DRW 19-OCT-84 11:00		NEXT HIGHER ASSEMBLY: D-DD-L0201-0		SIZE D	CODE BD
FIRST USED ON OPTION/MODEL:				NUMBER L0201-0-CSL5	REV. A

2216

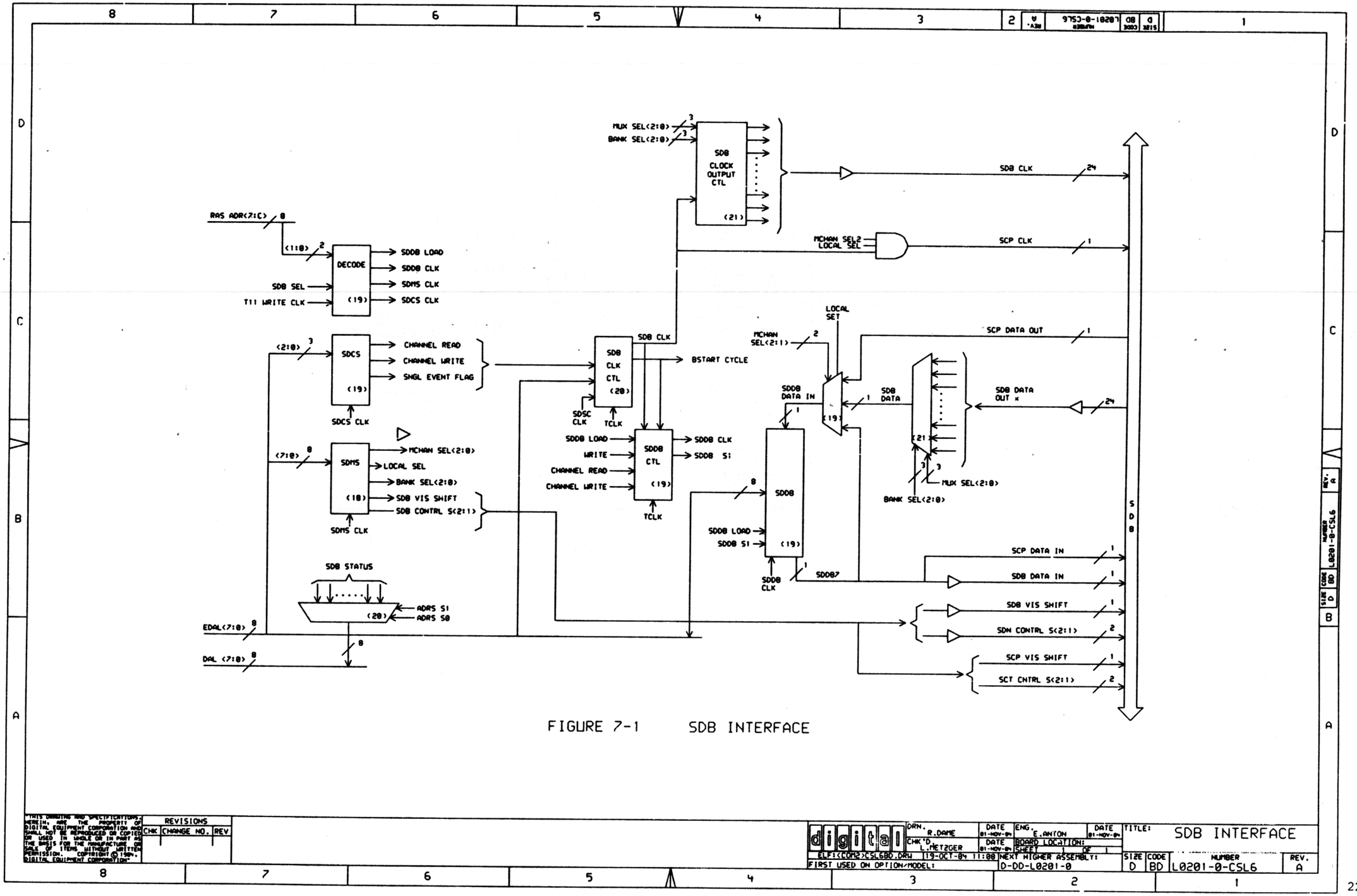
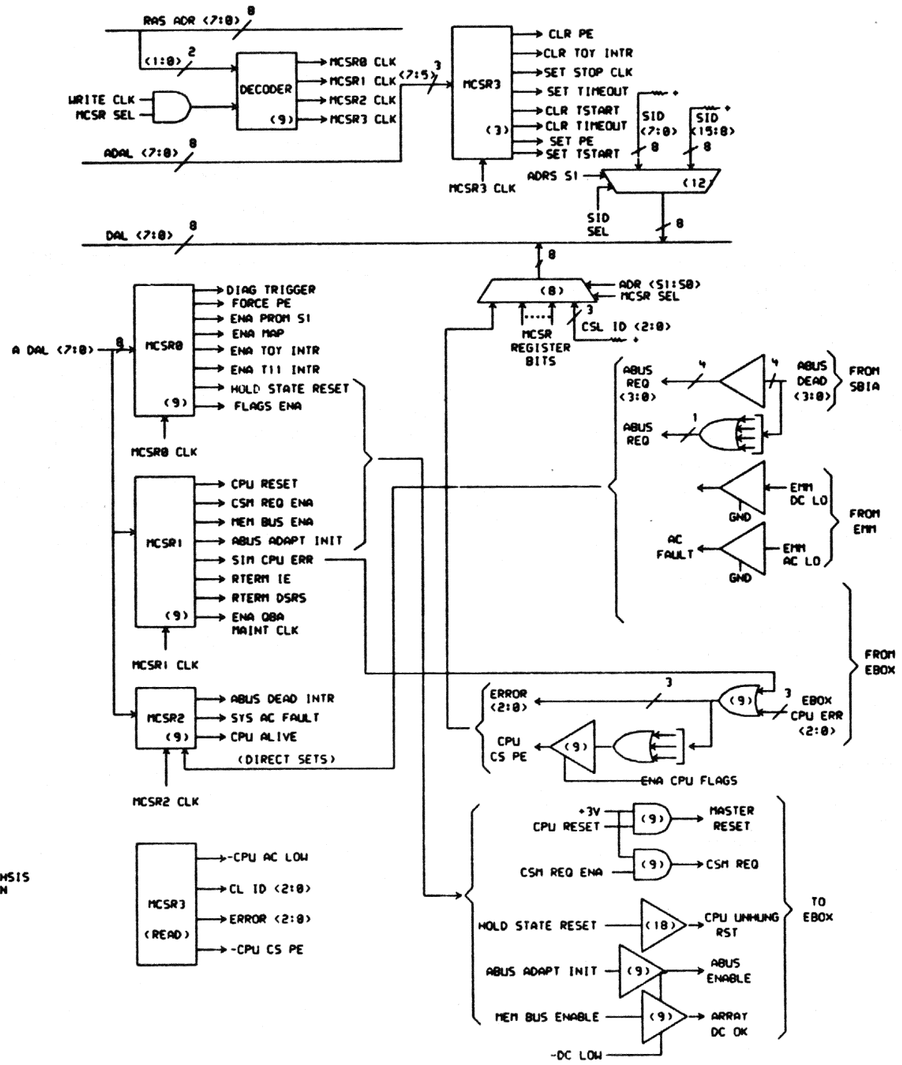


FIGURE 7-1 SDB INTERFACE

REVISIONS		
CHK	CHANGE NO.	REV

DRN. R.DAME	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84	TITLE: SDB INTERFACE	
CHK'D L.METZGER	DATE 01-NOV-84	BOARD LOCATION: SHEET 1 OF 1			
ELF1<COM2>CSL6BD.DRW 19-OCT-84 11:08		NEXT HIGHER ASSEMBLY: D-DD-L0201-0		SIZE D / CODE BD / NUMBER L0201-0-CSL6 / REV. A	
FIRST USED ON OPTION/MODEL:					



NOTE: NUMBERS IN PARENTHSIS INDICATE PRINT PREFIX IN ENGINEERING PRINT SET

FIGURE 8-1 MISCELLANEOUS CONTROL/STATUS LOGIC

REVISIONS		
CHK	CHANGE NO.	REV

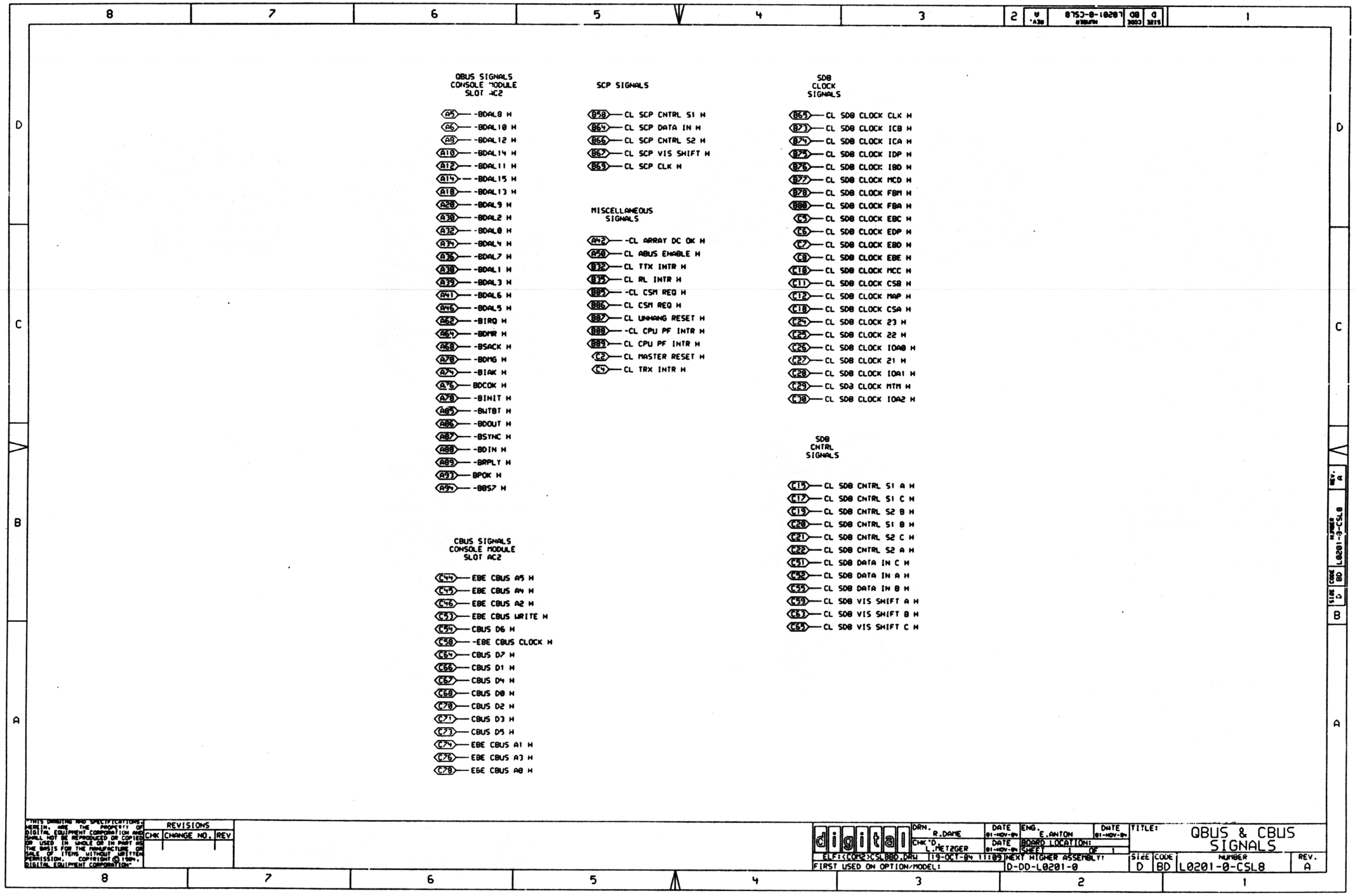
digital

DRN. R.DAME — DATE 01-NOV-84
CHK'D L.METZGER — DATE 01-NOV-84
ENG. E.ANTON — DATE 01-NOV-84
ELF:<COM2>CSL7BD.DRW 23-OCT-84 10:05
BOARD LOCATIONS:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
D-DD-L0201-0

TITLE: MISCELLANEOUS CNTRL/STATUS LOGIC

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL7	A

2218


QBUS SIGNALS
CONSOLE MODULE
SLOT AC2
A5 -BDAL8 H
A6 -BDAL10 H
A9 -BDAL12 H
A10 -BDAL14 H
A12 -BDAL11 H
A14 -BDAL15 H
A18 -BDAL13 H
A20 -BDAL9 H
A30 -BDAL2 H
A32 -BDAL0 H
A34 -BDAL4 H
A36 -BDAL7 H
A38 -BDAL1 H
A39 -BDAL3 H
A41 -BDAL6 H
A46 -BDAL5 H
A62 -BIRQ H
A64 -BDMR H
A68 -BSACK H
A70 -BDMG H
A74 -BIAK H
A75 BDCOK H
A78 -BINIT H
A85 -BWTBT H
A86 -BDOUT H
A87 -BSYNC H
A88 -BDIN H
A89 -BRPLY H
A93 BPOK H
A94 -BBS7 H
CBUS SIGNALS
CONSOLE MODULE
SLOT AC2
C44 EBE CBUS A5 H
C45 EBE CBUS A4 H
C46 EBE CBUS A2 H
C53 EBE CBUS WRITE H
C54 CBUS D6 H
C58 -EBE CBUS CLOCK H
C64 CBUS D7 H
C66 CBUS D1 H
C67 CBUS D4 H
C68 CBUS D0 H
C70 CBUS D2 H
C71 CBUS D3 H
C73 CBUS D5 H
C74 EBE CBUS A1 H
C76 EBE CBUS A3 H
C78 EBE CBUS A0 H
SCP SIGNALS
B58 CL SCP CNTRL S1 H
B64 CL SCP DATA IN H
B65 CL SCP CNTRL S2 H
B67 CL SCP VIS SHIFT H
B69 CL SCP CLK H
MISCELLANEOUS SIGNALS
A42 -CL ARRAY DC OK H
A50 CL ABUS ENABLE H
B32 CL TTX INTR H
B35 CL RL INTR H
B85 -CL CSM REQ H
B86 CL CSM REQ H
B87 CL UNHANG RESET H
B88 -CL CPU PF INTR H
B89 CL CPU PF INTR H
C2 CL MASTER RESET H
C4 CL TRX INTR H
SDB CLOCK SIGNALS
B65 CL SDB CLOCK CLK H
B73 CL SDB CLOCK ICB H
B74 CL SDB CLOCK ICA H
B75 CL SDB CLOCK IDP H
B76 CL SDB CLOCK IBD H
B77 CL SDB CLOCK MCD H
B78 CL SDB CLOCK FBM H
B80 CL SDB CLOCK FBA H
C5 CL SDB CLOCK EBC H
C6 CL SDB CLOCK EDP H
C7 CL SDB CLOCK EBD H
C8 CL SDB CLOCK EBE H
C10 CL SDB CLOCK MCC H
C11 CL SDB CLOCK CSB H
C12 CL SDB CLOCK MAP H
C18 CL SDB CLOCK CSA H
C24 CL SDB CLOCK 23 H
C25 CL SDB CLOCK 22 H
C26 CL SDB CLOCK IOA0 H
C27 CL SDB CLOCK 21 H
C28 CL SDB CLOCK IOA1 H
C29 CL SDB CLOCK MTM H
C30 CL SDB CLOCK IOA2 H
SDB CNTRL SIGNALS
C15 CL SDB CNTRL S1 A H
C17 CL SDB CNTRL S1 C H
C19 CL SDB CNTRL S2 B H
C20 CL SDB CNTRL S1 B H
C21 CL SDB CNTRL S2 C H
C22 CL SDB CNTRL S2 A H
C51 CL SDB DATA IN C H
C52 CL SDB DATA IN A H
C55 CL SDB DATA IN B H
C59 CL SDB VIS SHIFT A H
C61 CL SDB VIS SHIFT B H
C63 CL SDB VIS SHIFT C H
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REVISIONS
CHK CHANGE NO. REV
digital
DRN. R.DAME DATE 01-NOV-84
CHK'D L.METZGER DATE 01-NOV-84
ENG. E.ANTON DATE 01-NOV-84
BOARD LOCATION: SHEET 1 OF 1
ELF:<COM2>CSL88D.DRW 19-OCT-84 11:09
NEXT HIGHER ASSEMBLY: D-DD-L0201-0
FIRST USED ON OPTION/MODEL:
TITLE: QBUS & CBUS SIGNALS
SIZE D CODE BD NUMBER L0201-0-CSL8 REV. A

[redacted]

SID

J9

J91101	CL ID2 H	1	2	GND	
J91103	CL ID1 H	3	4	GND	
J91105	CL ID0 H	5	6	GND	
J91107	NC	7	8	GND	
J91109	NC	9	10	GND	
J91111	NC	11	12	GND	
J91113	NC	13	14	GND	
J91115	NC	15	16	GND	
J91117	SID23 H	17	18	GND	
J91119	SID22 H	19	20	GND	
J91121	SID21 H	21	22	GND	
J91123	SID20 H	23	24	GND	
J91125	SID19 H	25	26	GND	
J91127	SID18 H	27	28	GND	
J91129	SID17 H	29	30	GND	
J91131	SID16 H	31	32	GND	
J91133	SID15 H	33	34	GND	
J91135	SID14 H	35	36	GND	
J91137	SID13 H	37	38	GND	
J91139	SID12 H	39	40	GND	
J91141	SID11 H	41	42	GND	
J91143	SID10 H	43	44	GND	
J91145	SID09 H	45	46	GND	
J91147	SID06 H	47	48	GND	
J91149	SID07 H	49	50	GND	
J91151	SID06 H	51	52	GND	
J91153	SID05 H	53	54	GND	
J91155	SID04 H	55	56	GND	
J91157	SID03 H	57	58	GND	
J91159	SID02 H	59	60	GND	
J91161	SID01 H	61	62	GND	
J91163	SID00 H	63	64	GND	
J91165	NC	65	66	GND	
J91167	NC	67	68	GND	
J91169	NC	69	70	GND	
J91171	NC	71	72	GND	
J91173	NC	73	74	GND	
J91175	NC	75	76	GND	
J91177	NC	77	78	GND	
J91179	NC	79	80	GND	
J91181	NC	81	82	GND	
J91183	NC	83	84	GND	
J91185	NC	85	86	GND	
J91187	NC	87	88	GND	
J91189	NC	89	90	GND	
		91	92	GND	
J91193	ENA H	93	94	GND	

J9

FROM MPS/EMM

J12

J12101	EMM BUS B L	1	2	EMM BUS A L	J12102
J12103	SERIAL KEY SOURCE H	3	4	SERIAL KEY SENSE H	J12104
J12105	PARALLEL KEY SOURCE H	5	6	PARALLEL KEY SENSE H	J12106
J12107	EMM3 CPU AC LO L	7	8	(B,CPU AC LO RTN L,GND)	J12108
J12109	EMM3 CPU DC LO L	9	10	(B,CPU DC LO RTN L,GND)	J12110
J12111	EMM3 SBIA AC LO L	11	12	(B,SBIA AC LO RTN L,GND)	J12112
J12113	EMM3 SBIA DC LO L	13	14	(B,SBIA DC LO RTN L,GND)	J12114
J12115	EMM3 ARRAY +5V OK L	15	16	(B,ARRAY +5V OK RTN L,GND)	J12116
J12117	EMM MODULE A OK H	17	18	(B,MODULE A RTN L,GND)	J12118
J12119	NC	19	20	NC	

J12

TO CSL/EMM PANEL

J10

GND	1	2	-BRXDB H	J10102	
GND	3	4	-BTXDB H	J10104	
GND	5	6	-CRXDB H	J10106	
GND	7	8	CDSR H	J10108	
GND	9	10	CCTS H	J10110	
GND	11	12	CDCD H	J10112	
GND	13	14	-CTXDB H	J10114	
GND	15	16	CRIS H	J10116	
GND	17	18	CDTR H	J10118	
GND	19	20	-CDSRS H	J10120	
GND	21	22	NC	J10122	
GND	23	24	NC	J10124	
GND	25	26	NC	J10126	
GND	27	28	NC	J10128	
GND	29	30	NC	J10130	
GND	31	32	NC	J10132	
GND	33	34	NC	J10134	
GND	35	36	NC	J10136	
GND	37	38	NC	J10138	
GND	39	40	NC	J10140	

J10

QBUS

J7

GND	1	2	NC	J7102	
GND	3	4	-BDAL0 H	J7104	
GND	5	6	-BDAL1 H	J7106	
GND	7	8	-BDAL2 H	J7108	
GND	9	10	-BDAL3 H	J7110	
GND	11	12	-BDAL4 H	J7112	
GND	13	14	-BDAL5 H	J7114	
GND	15	16	-BDAL6 H	J7116	
GND	17	18	-BDAL7 H	J7118	
GND	19	20	-BDAL8 H	J7120	
GND	21	22	-BDAL9 H	J7122	
GND	23	24	-BDAL10 H	J7124	
GND	25	26	-BDAL11 H	J7126	
GND	27	28	-BDAL12 H	J7128	
GND	29	30	-BDAL13 H	J7130	
GND	31	32	-BDAL14 H	J7132	
GND	33	34	-BDAL15 H	J7134	
GND	35	36	-BUTBT H	J7136	
GND	37	38	-BBS7 H	J7138	
GND	39	40	GND	J7140	

J7

TO SCP

J11

GND	1	2	CL SCP DATA IN H	J11102	
GND	3	4	CL SCP CLK H	J11104	
GND	5	6	SCP DATA OUT H	J11106	
GND	7	8	CL SCP CNTRL S1 H	J11108	
GND	9	10	CL SCP CNTRL S2 H	J11110	
GND	11	12	-CLBI D INIT H	J11112	
GND	13	14	CL SCP VIS SHIFT H	J11114	
GND	15	16	NC	J11116	
GND	17	18	NC	J11118	
GND	19	20	NC	J11120	

J11

J8

GND	1	2	NC	J8102	
GND	3	4	-BDOUT H	J8104	
GND	5	6	-BRPLY H	J8106	
GND	7	8	-BDIN H	J8108	
GND	9	10	-BSYNC H	J8110	
GND	11	12	-BIRQ H	J8112	
GND	13	14	-BIAK H	J8114	
GND	15	16	-BDMR H	J8116	
GND	17	18	-BDMG H	J8118	
GND	19	20	-BINIT H	J8120	
GND	21	22	NC	J8122	
GND	23	24	NC	J8124	
GND	25	26	NC	J8126	
GND	27	28	NC	J8128	
GND	29	30	BDCOK H	J8130	
GND	31	32	BPOK H	J8132	
GND	33	34	NC	J8134	
GND	35	36	-BSACK H	J8136	
GND	37	38	NC	J8138	
GND	39	40	NC	J8140	

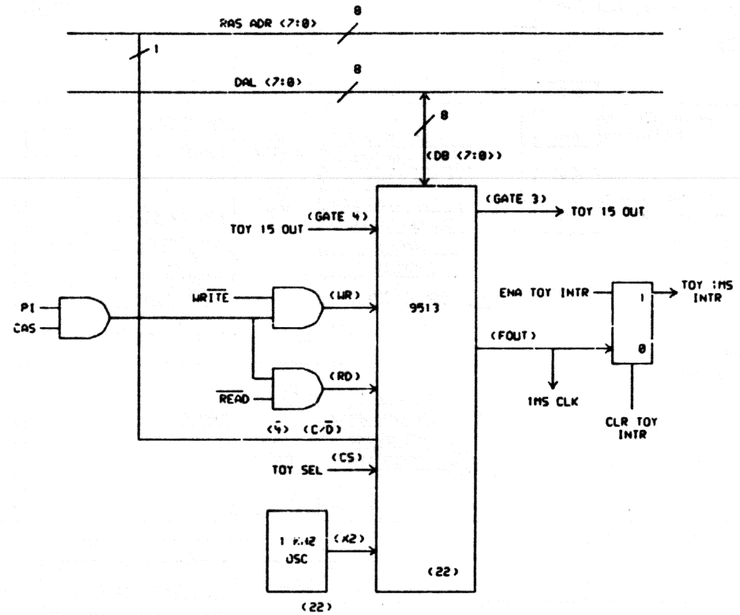
J8

REVISIONS		
CHK	CHANGE NO.	REV

DRN. R.DANE	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84
CHK D. L.METZGER	DATE 01-NOV-84	BOARD LOCATION:	
ELF:[COM2.CSL9BD.DRV] 19-OCT-84 11:09		SHEET 1 OF 1	
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-L0201-0	

TITLE: CONSOLE BP CONNECTORS

SIZE	CODE	NUMBER	REV.
D	BD	L0201-0-CSL9	A



NOTE : NUMBERS IN PARENTHESIS INDICATE PRINT PREFIX IN ENGINEERING PRINT SET

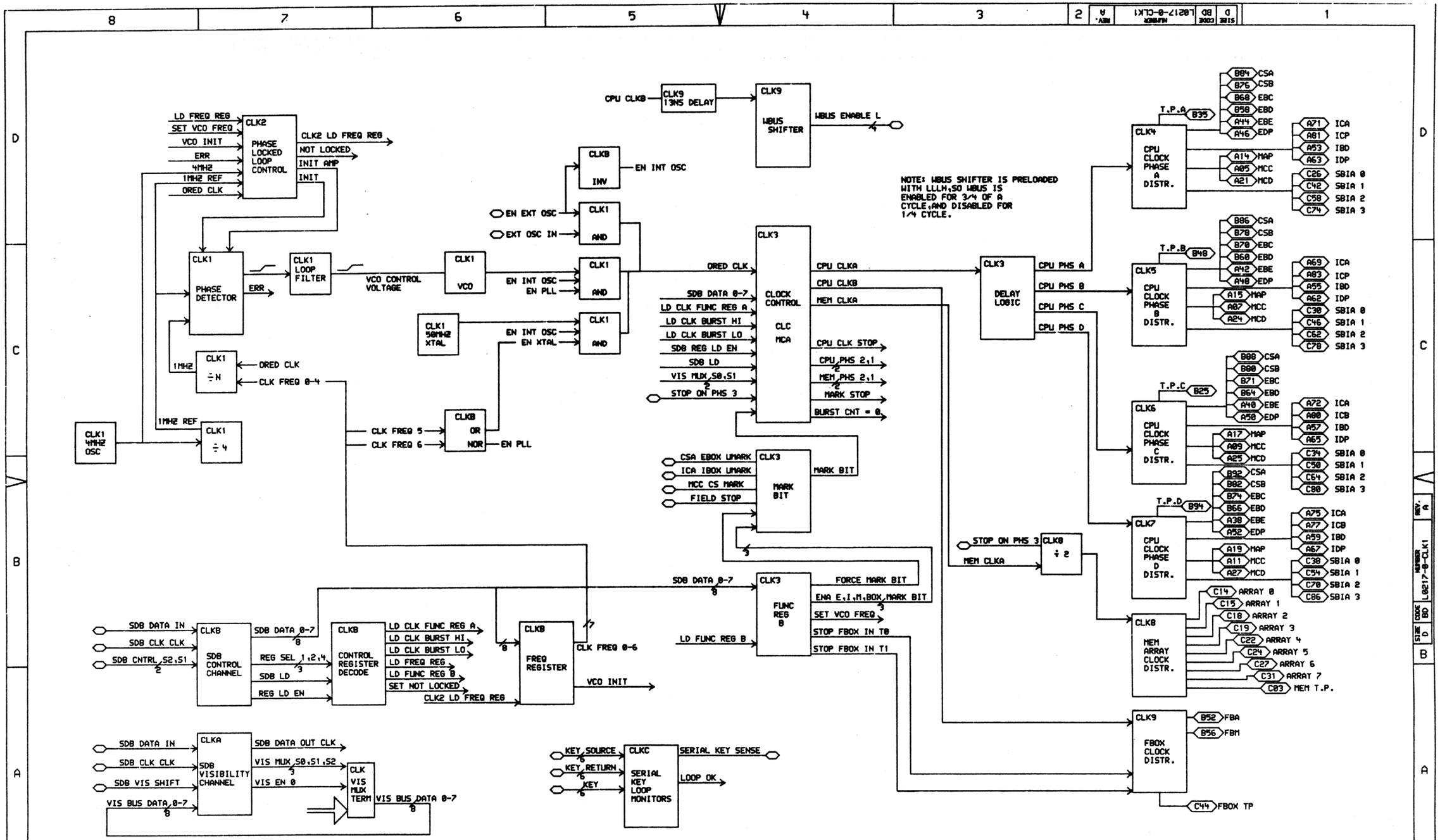
FIGURE 5-1 TOY CLOCK CONTROLLER

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. R.DAME	DATE 01-NOV-84	ENG. E.ANTON	DATE 01-NOV-84	TITLE: TOY CLOCK CONTROLLER	
CHK'D L.METZGER	DATE 01-NOV-84	BOARD LOCATION: SHEET 1 OF 1			
E.L.P.:(COM2)CSLABD.DRW 19-OCT-84 11:09		NEXT HIGHER ASSEMBLY: D-DD-L0201-0		SIZE D	CODE BD
FIRST USED ON OPTION/MODEL:				NUMBER L0201-0-CSLA	REV. A

2221



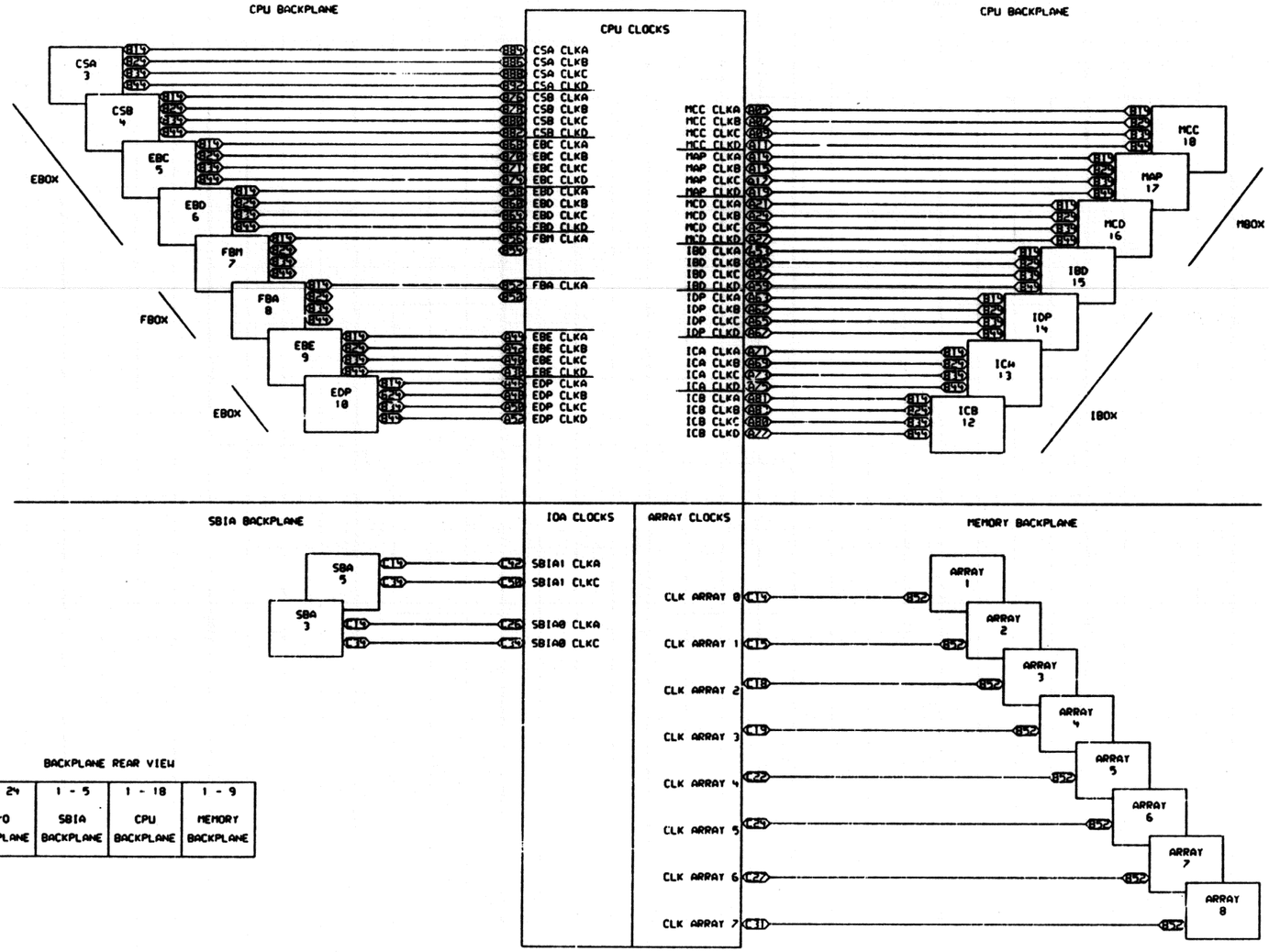
REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. ROGER B. DAME	DATE 18-DEC-84	ENG. S.DELAHUNT	DATE 18-DEC-84	TITLE: CLOCK MODULE BLK DIAGRAM	
CHK "D. L.METZGER"	DATE 18-DEC-84	BOARD LOCATION:	SHEET 1 OF 1		
VENCP1:<CLKC.SBM>CLK1BD.DAV 24-OCT-84 13:50		NEXT HIGHER ASSEMBLY: D-DD-L0217-0		SIZE D	CODE BD
FIRST USED ON OPTION/MODEL:				NUMBER L0217-0-CLK1	REV. A

2222

CLK SLOT 11



BACKPLANE REAR VIEW

1 - 24	1 - 5	1 - 18	1 - 9
I/O BACKPLANE	SBIA BACKPLANE	CPU BACKPLANE	MEMORY BACKPLANE

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. R.DAME — DATE 09-NOV-84 — ENG. S.DELAHUNT — DATE 09-NOV-84

CHK'D L.METZGER — DATE 09-NOV-84 — BOARD LOCATION: — SHEET 1 OF 1

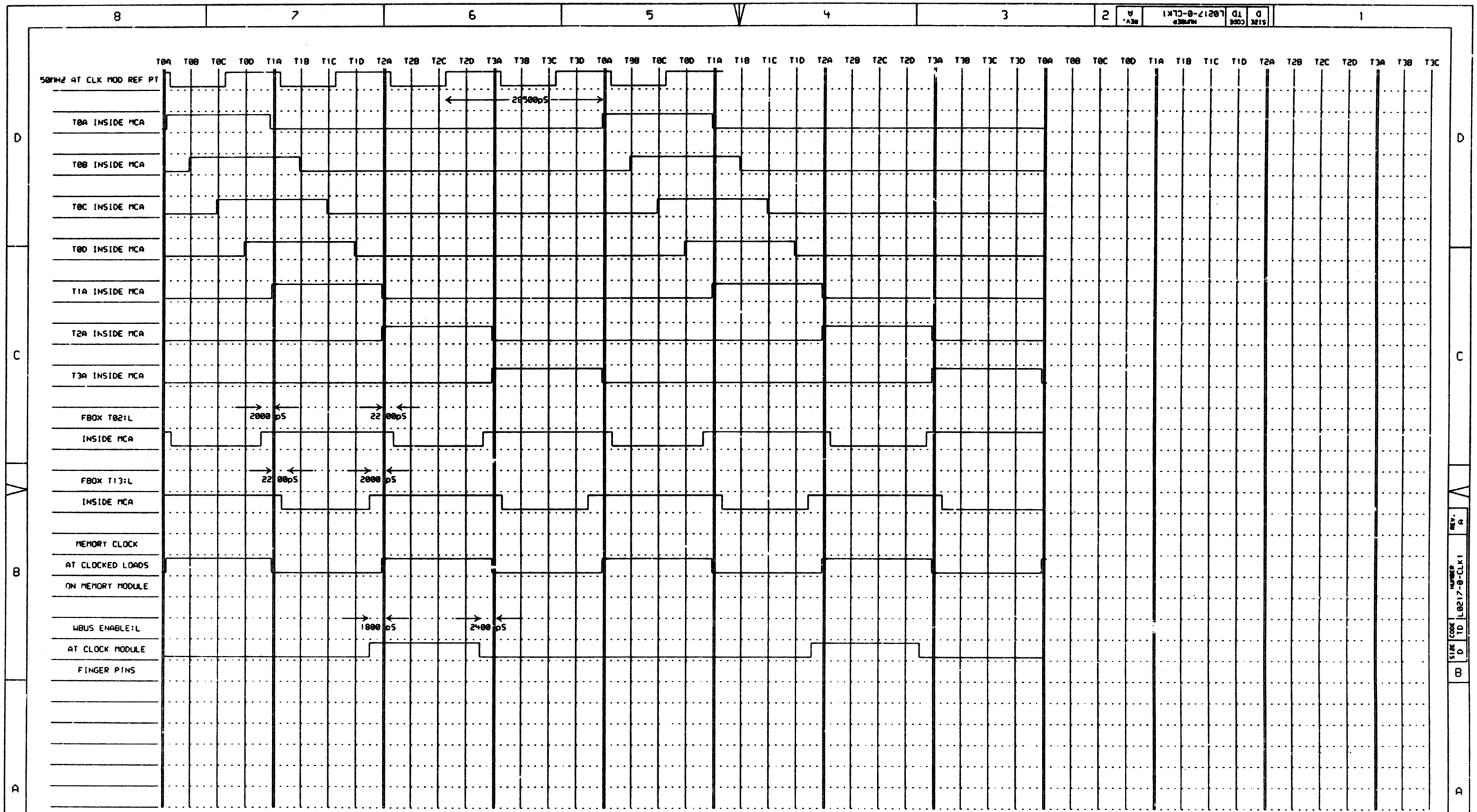
ELF:<BOWEN>CLK2BD.DRW 24-OCT-84 09:10 — NEXT HIGHER ASSEMBLY: D-DD-L0217-0

FIRST USED ON OPTION/MODEL:

TITLE: CLOCK I/O PIN CONNECTIONS

SIZE	CODE	NUMBER	REV.
D	BD	L0217-0-CLK2	A

2223



NOTE1: THE PRESENT CYCLE TIME (T0A TO T0A) IS 80nS.
NOTE2: THE ABOVE FIGURES ARE ROUNDED TO THE NEAREST 100 pS.
NOTE3: (T1-T3)X(B-D) ARE NOT SHOWN: THEY ARE IMPLICIT.
NOTE4: THE ABOVE FIGURES ARE NOMINAL. SKEW IS NOT REPRESENTED.

REVISIONS		
CHK	CHANGE NO.	REV

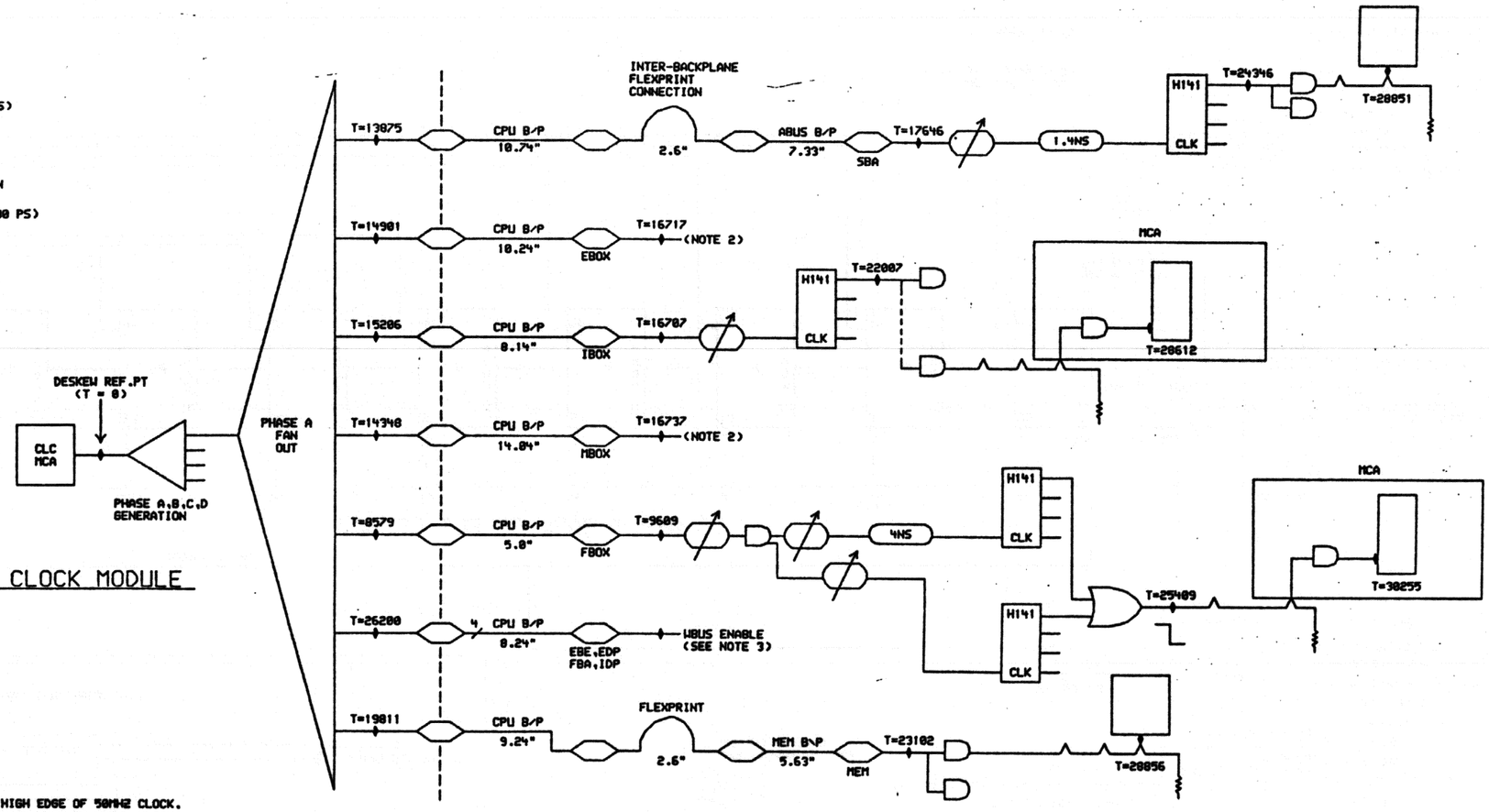
digital

DRN. "C.CAIAZZI"	DATE 09-NOV-84	ENG. "S.DELAMUNT"	DATE 09-NOV-84	TITLE: CLOCK PHASES	
CHK "D. L.METZGER"	DATE 09-NOV-84	BOARD LOCATION: SHEET 1 OF 1			
ELF:<BOWEN>CLK1TD.DRW 24-OCT-84 07:31		NEXT HIGHER ASSEMBLY: D-DD-L0217-0		SIZE D	CODE TD
FIRST USED ON OPTION/MODEL:				NUMBER L0217-0-CLK1	REV. A

2224

NOTE 1: THIS DIAGRAM SHOWS THE RELATIONSHIPS BETWEEN THE NOMINAL TIMES OF THE CLOCKS AT VARIOUS POINTS IN THE SYSTEM ALL TIMES ARE SHOWN IN PS (PICO SECONDS)

NOTE 2: ALL OF THE EBOX, IBOX, AND MBOX MODULES HAVE SIMILAR CLOCK DISTRIBUTION LOGIC. THE DESKEW TARGET VALUE FOR EACH OF THESE MODULES IS IDENTICAL (5300 PS)



CLOCK MODULE

NOTE 3: EACH OF THE 4 WBUS MODULES RECEIVES AN INDIVIDUAL COPY OF THE WBUS ENABLE FROM THE CLOCK MODULE. THE WBUS ENABLE IS NOT DESKEWED ON THE LOGIC MODULES.

NOTE 4: TIMES AT CLOCK MODULE FINGER PINS ARE HIGH EDGE OF 50MHZ CLOCK.
TIMES AT LOGIC MODULE FINGER PINS ARE HIGH EDGE OF 50MHZ CLOCK.

TIMES AT OTHER POINTS ON E/I/M BOX MODULES ARE FOR LEADING EDGE OF T0A CLOCK.

TO CALCULATE THE TIMES FOR T0B,T0C AND T0D, ADD 4545PS,9091PS AND 13636PS RESPECTIVELY TO THE TIMES SHOWN FOR T0A.

TIMES AT OTHER POINTS ON FBOX MODULES ARE FOR LOW EDGE OF T02 CLOCK.

ALL TIMES SHOWN FOR MEMORY CLOCKS ARE FOR HIGH EDGE OF 25MHZ CLOCK.

REVISIONS		
CHK	CHANGE NO.	REV

digital

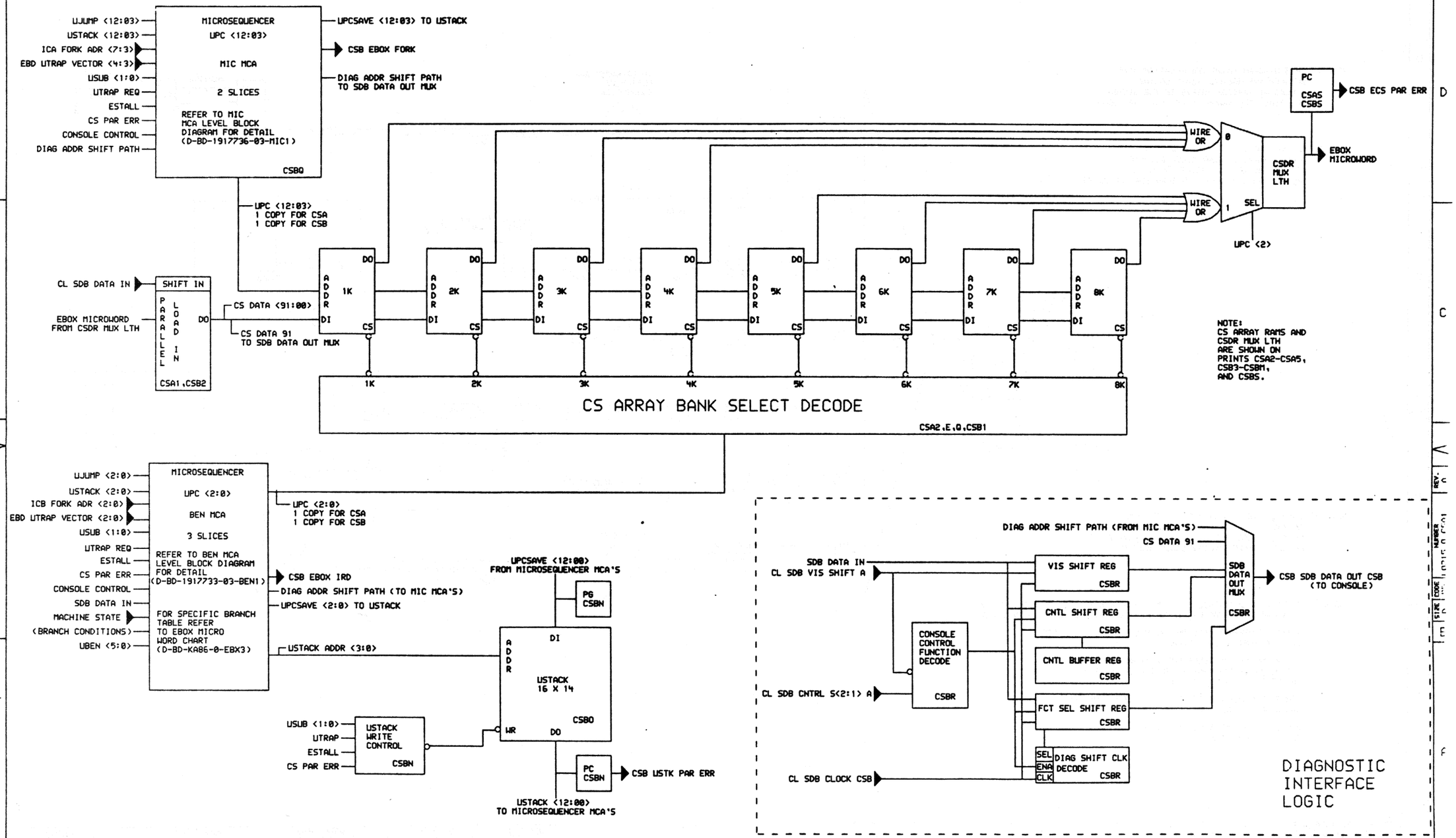
DRN: C.CAIAZZI
CHK'D: L.METZGER
DATE: 24-OCT-84
ENG: S.DELAHUNT
DATE: 24-OCT-84
DATE: 24-OCT-84
BOARD LOCATION:
SHEET 1 OF 1
VENCP1:<CLKG.SBM>CLK2TD.DRW 24-OCT-84 07:44
NEXT HIGHER ASSEMBLY: D-DD-L0217-0
FIRST USED ON OPTION/MODEL:

TITLE: CLOCK RELATIVE TIMES

SIZE	CODE	NUMBER	REV.
D	TD	L0217-0-CLK2	A

3 10/24

2225

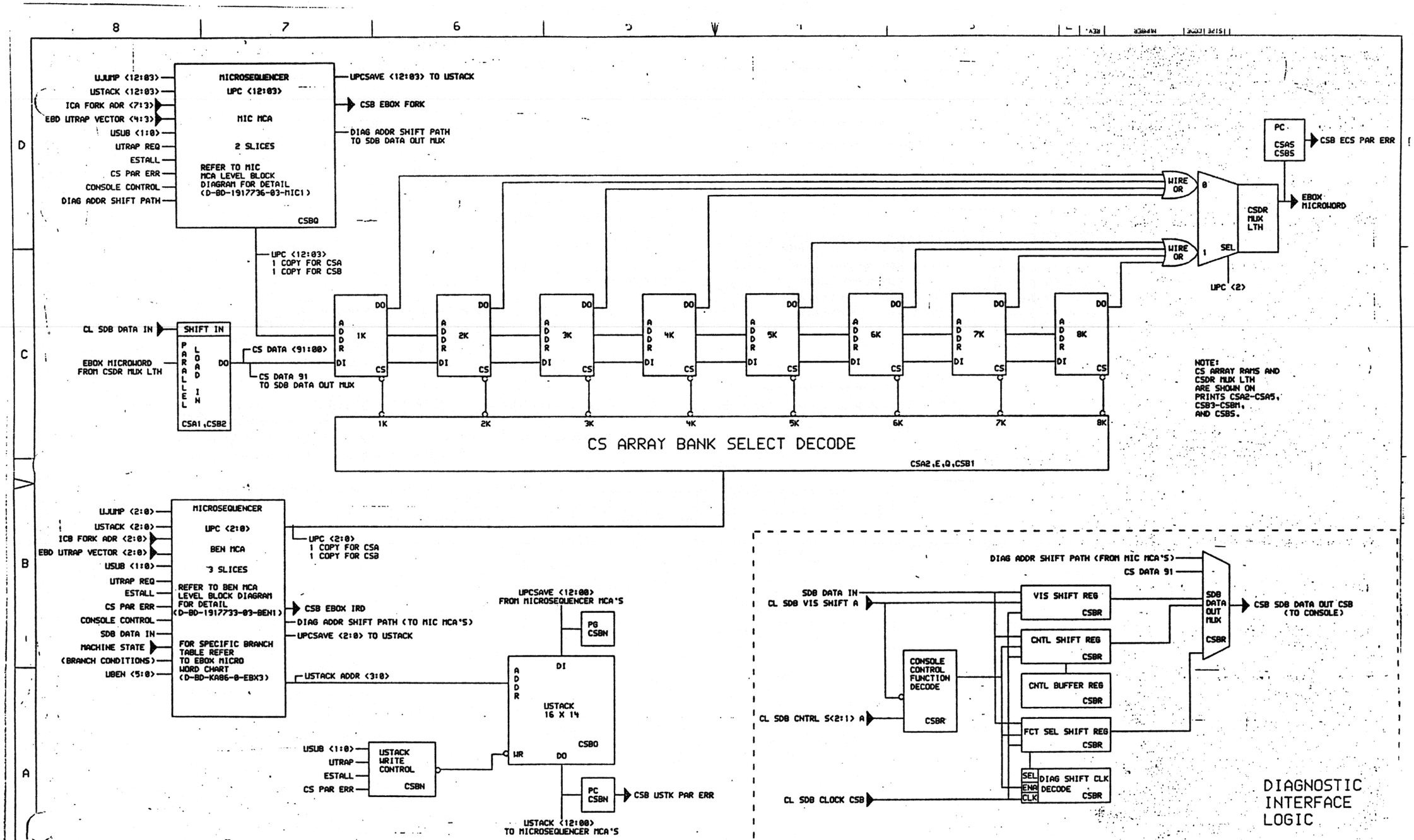


REVISIONS		
CHK	CHANGE NO.	REV

DRN. J.SMITH	DATE 21-SEP-84	ENG. B.HILLIARD	DATE 21-SEP-84
CHK D. L.METZGER	DATE 21-SEP-84	BOARD LOCATION: SHEET 1 OF 1	
VERSE2:(CSAB.SBM)CSA1BD.DRW 11-SEP-84 14:41		NEXT HIGHER ASSEMBLY: D-DD-L0215-0	
FIRST USED ON OPTION/MODEL:			

TITLE: MICROSEQUENCER BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0215-0-CSA1	A



REVISIONS		
CHK	CHANGE NO.	REV

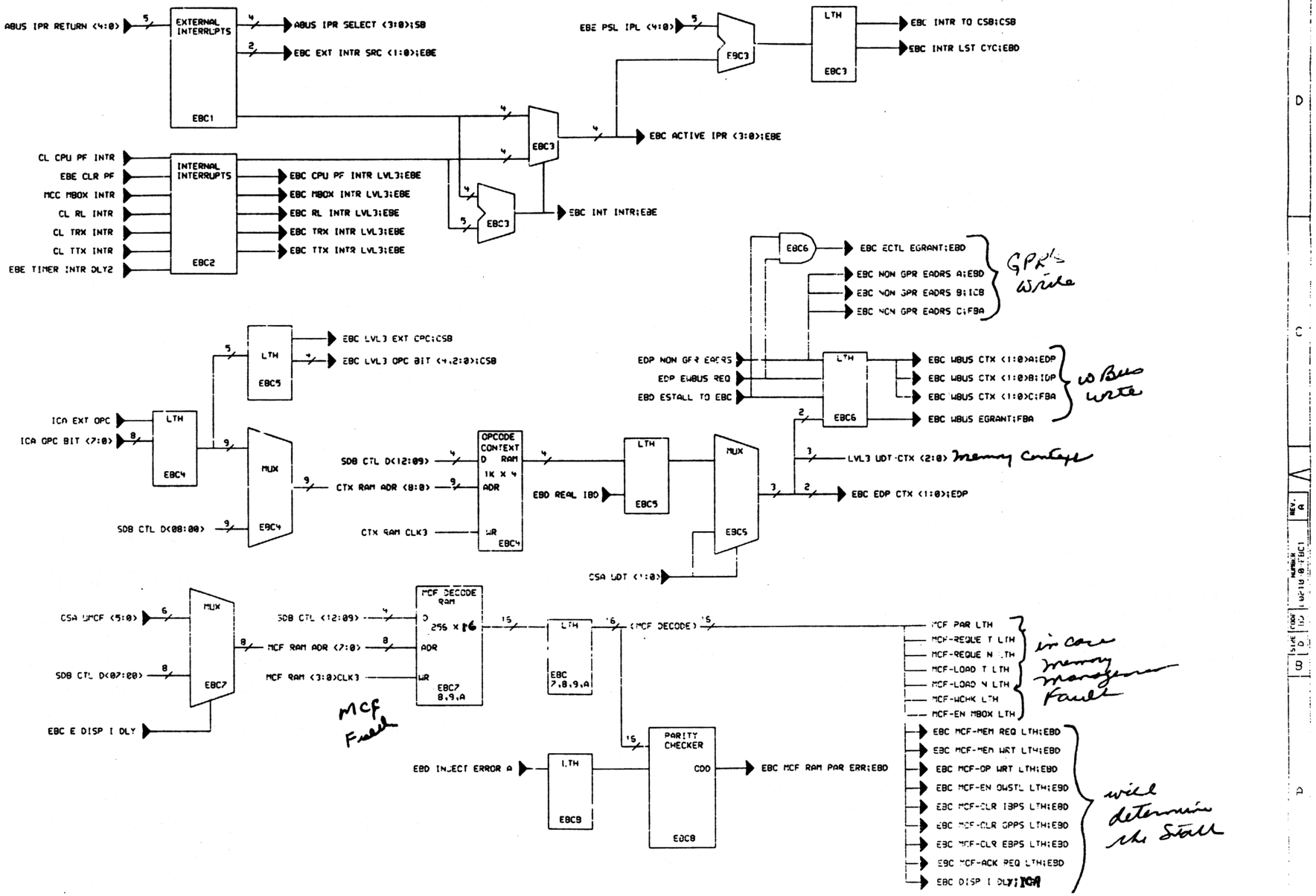
digital

DRN. J.SMITH — DATE 21-SEP-84
CHK'D L.METZGER — DATE 21-SEP-84
ENG. B.HILLIARD — DATE 21-SEP-84
BOARD LOCATION:
SHEET 1 OF
VENUS2:(CSBB,SBM)CSB1BD.DRW 13-SEP-84 07:04
NEXT HIGHER ASSEMBLY: D-DD-L0216-0
FIRST USED ON OPTION/MODEL:

TITLE: MICROSEQUENCER BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0216-0-CSB1	A

2227

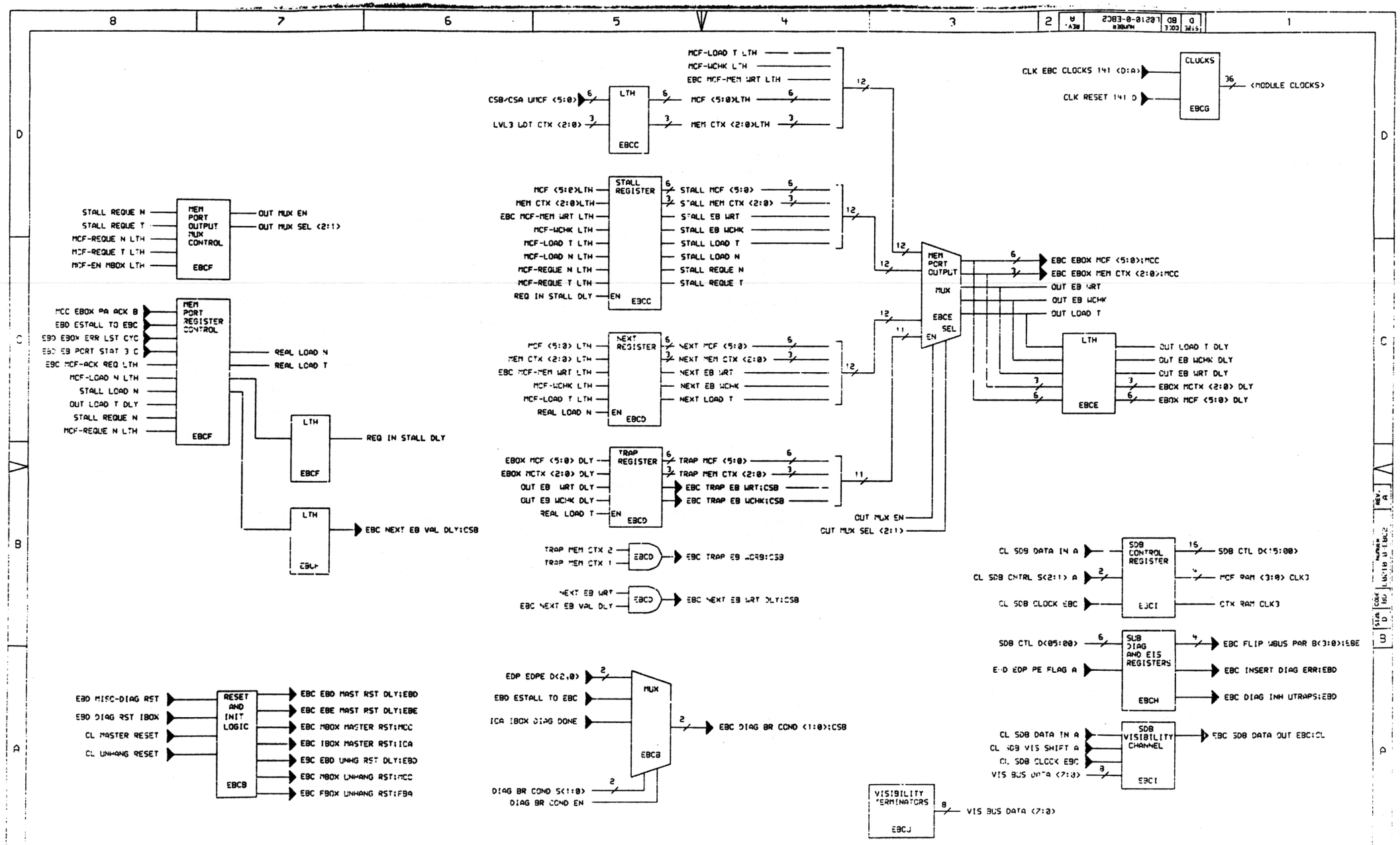


REVISIONS		
CHK	CHANGE NO.	REV

DRN: W.BOLAND	DATE 04-DEC-84	ENG: S.REICHERT	DATE 04-DEC-84
CHK'D: L.METZGER	DATE 04-DEC-84	APPROVAL:	
ELP:<CONT>EBC15D.DZW 03-JUL-84 10:25	SIZE: D	NEXT HIGHER ASSEMBLY: D-DD-L0210-0	
FIRST USED ON OPTION/MODEL:			

TITLE: BLOCK DIAGRAM EBC (L0210)

SIZE D | CODE 9D | NUMBER L0210-0-EBC1 | REV. A



REVISIONS		
CHK	CHANGE NO.	REV

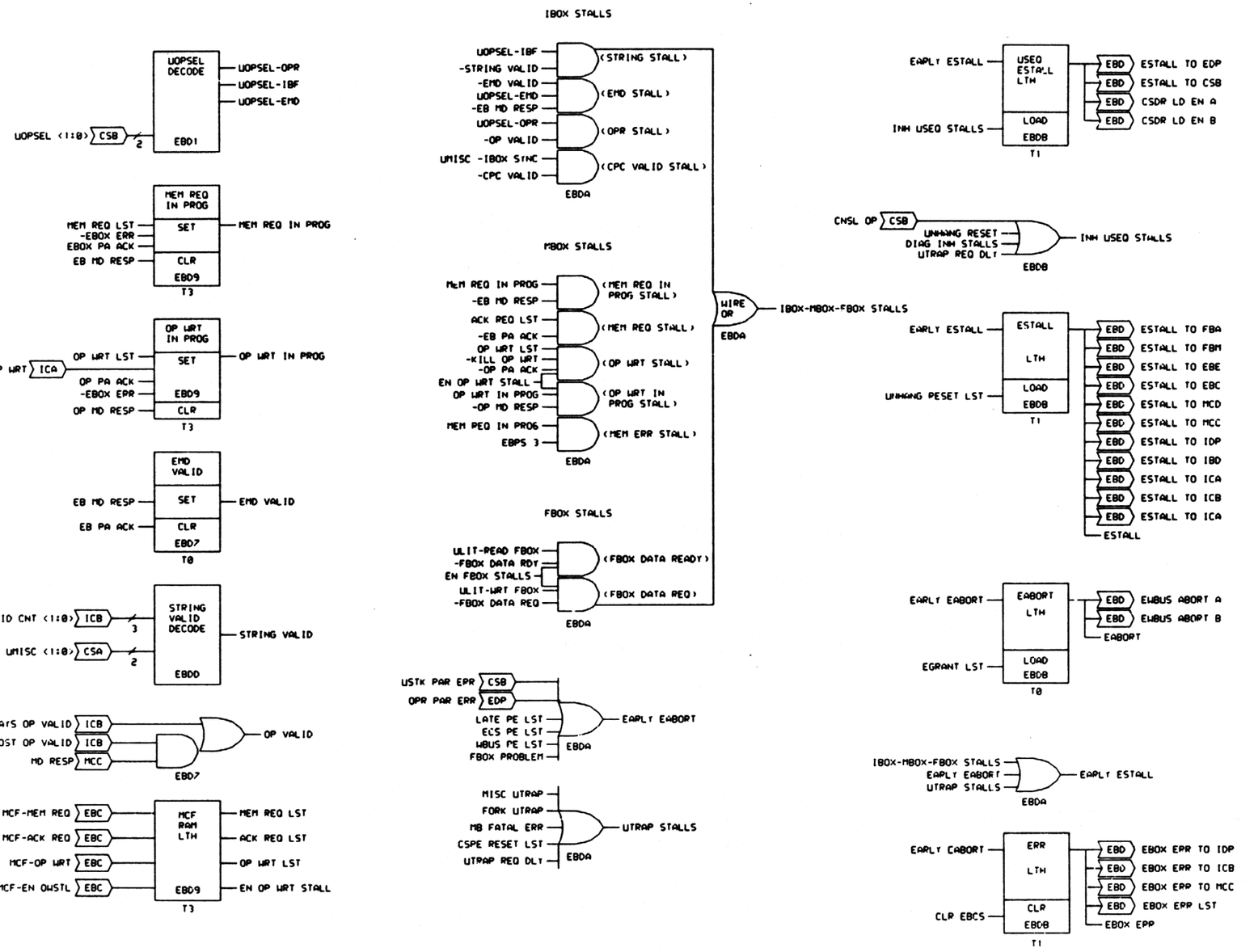
DRN. W.BOLAND — DATE 04-DEC-84 — ENG. S.RESCHER — DATE 04-DEC-84
CHK'D. L.METZGER — DATE 04-DEC-84 — BOARD LOCATION: — SHEET — OF
ELP:(CCM)SEB2280.DRW 03-JUL-84 10:25 NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: D-DD-L0210-0

TITLE: BLOCK DIAGRAM EBC (L0210)

SIZE	CODE	NUMBER	REV.
D	BD	L0210-0-EBC2	A

2229

41



REVISIONS		
CHK	CHANGE NO.	REV

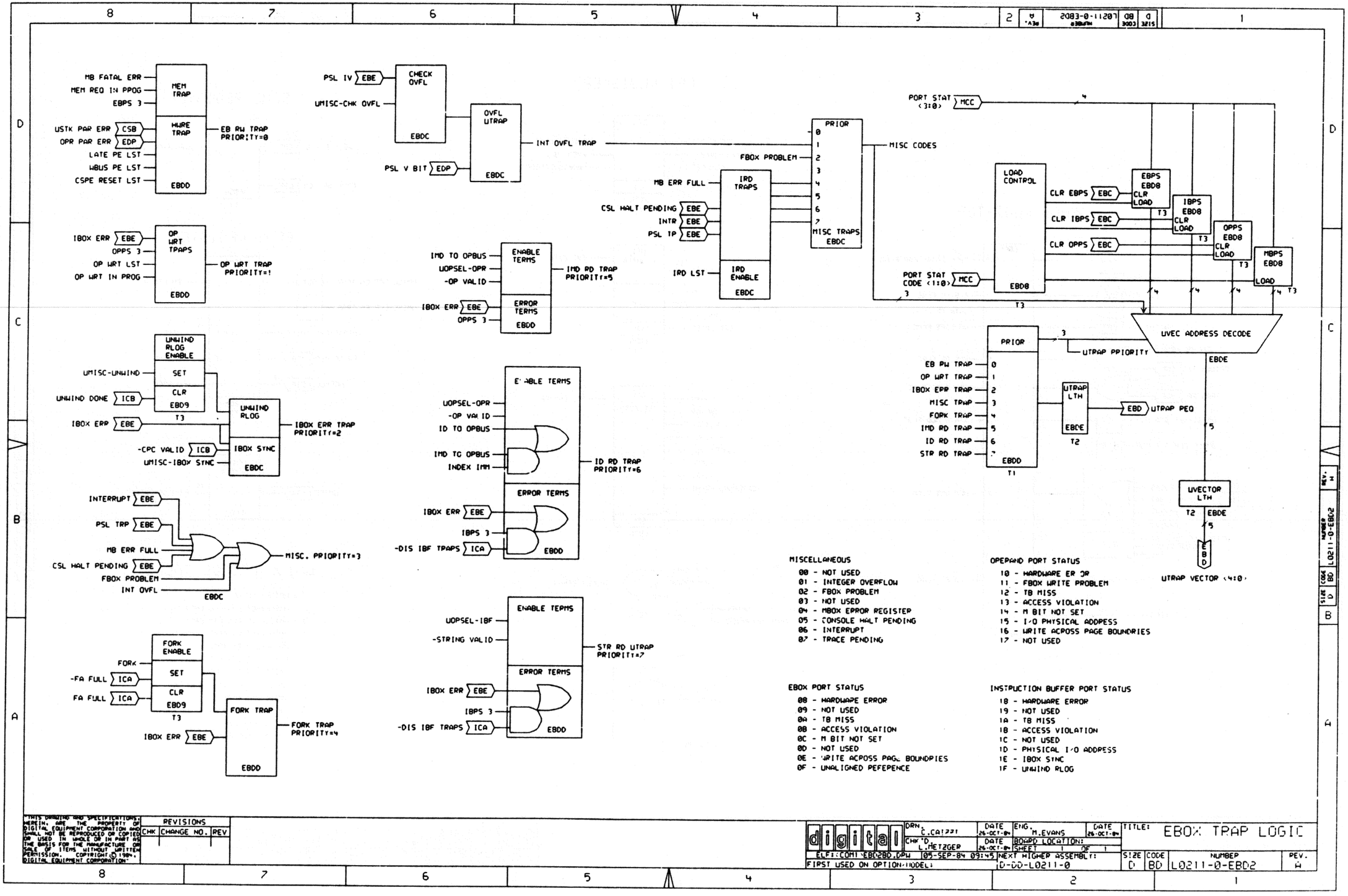
digital

DRN: C.CAIAZZI — DATE 26-OCT-84
CHK'D: L.METZGER — DATE 26-OCT-84
ENG: M.EVANS — DATE 26-OCT-84
BOMPD LOCATION:
SHEET 1 OF 1
ELF1:COM1-EBD1BD.DRW 05-SEP-84 09:47
NEXT HIGHER ASSEMBLY: D-DD-L0211-0
FIRST USED ON OPTION/MODEL:

TITLE: EBOX STALL AND ABORT LOGIC

SIZE	CODE	NUMBER	REV.
D	BD	L0211-0-EBD1	H

2230


MB FATAL ERR
MEM REQ IN PROG
EBPS 3
MEM TRAP
EBDD
USTK PAR ERR
OPR PAR ERR
LATE PE LST
WBUS PE LST
CSPE RESET LST
CSB
EDP
MWRE TRAP
EB RW TRAP PRIORITY=0
PSL IV
EBE
CHECK OVFL
EBDC
UMISC-CHK OVFL
OVFL UTRAP
INT OVFL TRAP
PSL V BIT
IBOX ERR
OPPS 3
OP WRT LST
OP WRT IN PROG
OP WRT TRAPS
OP WRT TRAP PRIORITY=1
IMD TO OPBUS
UOPSEL-OPR
-OP VALID
ENABLE TERMS
IMD RD TRAP PRIORITY=5
ERROR TERMS
UNWIND RLOG ENABLE
UMISC-UNWIND
SET
UNWIND DONE
ICB
CLR
EBD9
T3
UNWIND RLOG
IBOX ERR TRAP PRIORITY=2
-CPC VALID
IBOX SYNC
UMISC-IBOX SYNC
UOPSEL-OPR
-OP VALID
ID TO OPBUS
IMD TO OPBUS
INDEX IMM
ENABLE TERMS
ID RD TRAP PRIORITY=6
ERROR TERMS
IBOX ERR
IBPS 3
-DIS IBF TRAPS
ICA
EBDD
INTERRUPT
PSL TRP
MB ERR FULL
CSL HALT PENDING
FBOX PROBLEM
INT OVFL
MISC. PRIORITY=3
EBDC
FORK ENABLE
FORK
-FA FULL
FA FULL
SET
CLR
EBD9
T3
FORK TRAP
FORK TRAP PRIORITY=4
UOPSEL-IBF
-STRING VALID
ENABLE TERMS
STR RD UTRAP PRIORITY=7
ERROR TERMS
PRIOR
0
1
2
3
4
5
6
7
MISC TRAPS
EBDC
FBOX PROBLEM
MB ERR FULL
CSL HALT PENDING
INTR
PSL IP
IRD TRAPS
IRD LST
IRD ENABLE
MISC CODES
PORT STAT <3:0>
MCC
PORT STAT CODE <1:0>
LOAD CONTROL
EBD8
CLR EBPS
CLR IBPS
CLR OPPS
EBC
EBPS EBD8 CLR LOAD
IBPS EBD8 CLR LOAD
OPPS EBD8 CLR LOAD
MBPS EBD8 LOAD
T3
UVEC ADDRESS DECODE
EBDE
UTRAP PRIORITY
PRIOR
EB RW TRAP
OP WRT TRAP
IBOX ERR TRAP
MISC TRAP
FORK TRAP
IMD RD TRAP
ID RD TRAP
STR RD TRAP
EBDD
T1
UTRAP LTH
EBDE
T2
EBD
UTRAP PEQ
UVECTOR LTH
T2
EBDE
EBD
UTRAP VECTOR <4:0>
MISCELLANEOUS
00 - NOT USED
01 - INTEGER OVERFLOW
02 - FBOX PROBLEM
03 - NOT USED
04 - MBOX ERROR REGISTER
05 - CONSOLE HALT PENDING
06 - INTERRUPT
07 - TRACE PENDING
OPERAND PORT STATUS
10 - HARDWARE ER OR
11 - FBOX WRITE PROBLEM
12 - TB MISS
13 - ACCESS VIOLATION
14 - M BIT NOT SET
15 - I/O PHYSICAL ADDRESS
16 - WRITE ACROSS PAGE BOUNDRIES
17 - NOT USED
EBOX PORT STATUS
08 - HARDWARE ERROR
09 - NOT USED
0A - TB MISS
0B - ACCESS VIOLATION
0C - M BIT NOT SET
0D - NOT USED
0E - WRITE ACROSS PAGE BOUNDRIES
0F - UNALIGNED REFERENCE
INSTRUCTION BUFFER PORT STATUS
18 - HARDWARE ERROR
19 - NOT USED
1A - TB MISS
1B - ACCESS VIOLATION
1C - NOT USED
1D - PHYSICAL I/O ADDRESS
1E - IBOX SYNC
1F - UNWIND RLOG
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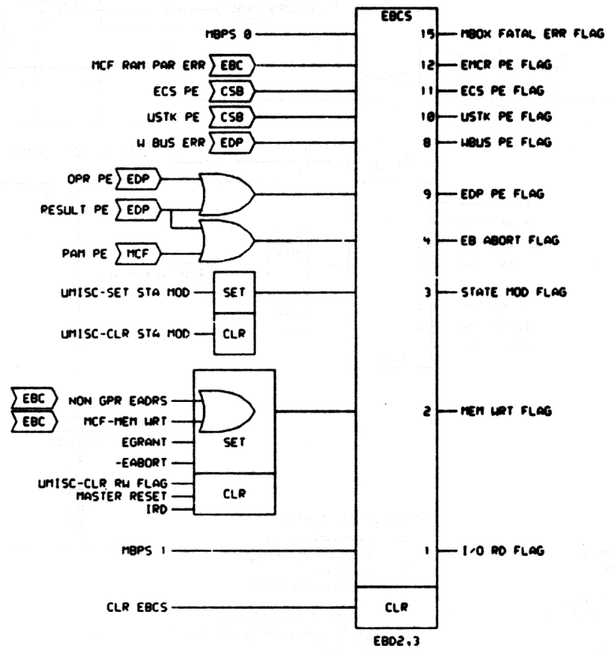
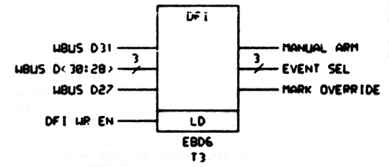
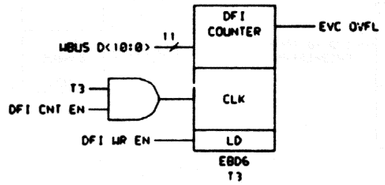
REVISIONS
CHK
CHANGE NO.
REV
digital
DRN C.CAIZZI
DATE 26-OCT-84
ENG. M.EVANS
DATE 26-OCT-84
CHK D.METZGER
DATE 26-OCT-84
BOARD LOCATION:
SHEET 1 OF 1
ELF::COMI'EBD2BD.DPW 05-SEP-84 09:45
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION-MODEL:
D-DD-L0211-0
TITLE: EBOX TRAP LOGIC
SIZE D
CODE BD
NUMBER L0211-0-EBD2
REV. A

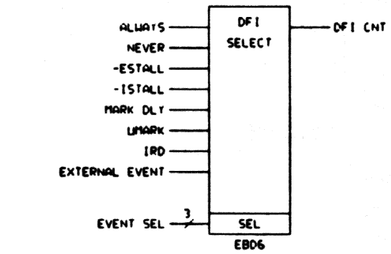
EBCS REGISTER

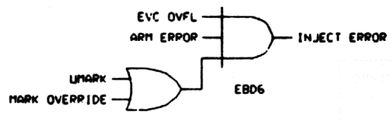


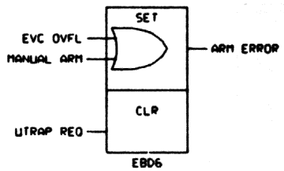
DFI REGISTER



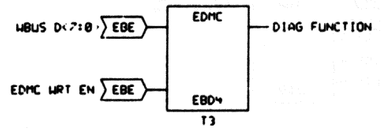




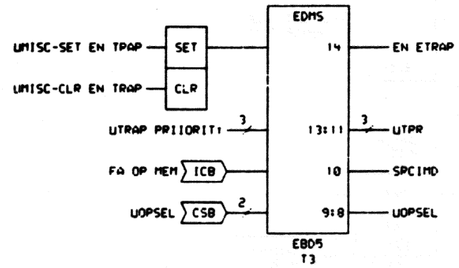


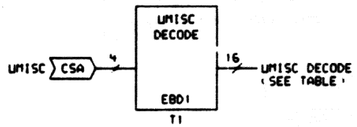


EDMC REGISTER



EDMS REGISTER





UMISC DECODE TABLE

1 - UMISC-CLR RW FLAG
2 - UMISC-SET FPD (TO EBE)
3 - UMISC-CLR FPD (TO EBE)
4 - UMISC-SET EN TRAP
5 - UMISC-CLR EN TRAP
6 - UMISC-SET STA MOD
7 - UMISC-CLR STA MOD
8 - UMISC-IBOX SYNC (TO IBOX)
C - UMISC-CHK OVFL
D - UMISC-UNWIND RLOG (TO IBOX)
E - UMISC-ENA FOPK
F - UMISC-DIAG RESET

REVISIONS		
CHK	CHANGE NO.	REV

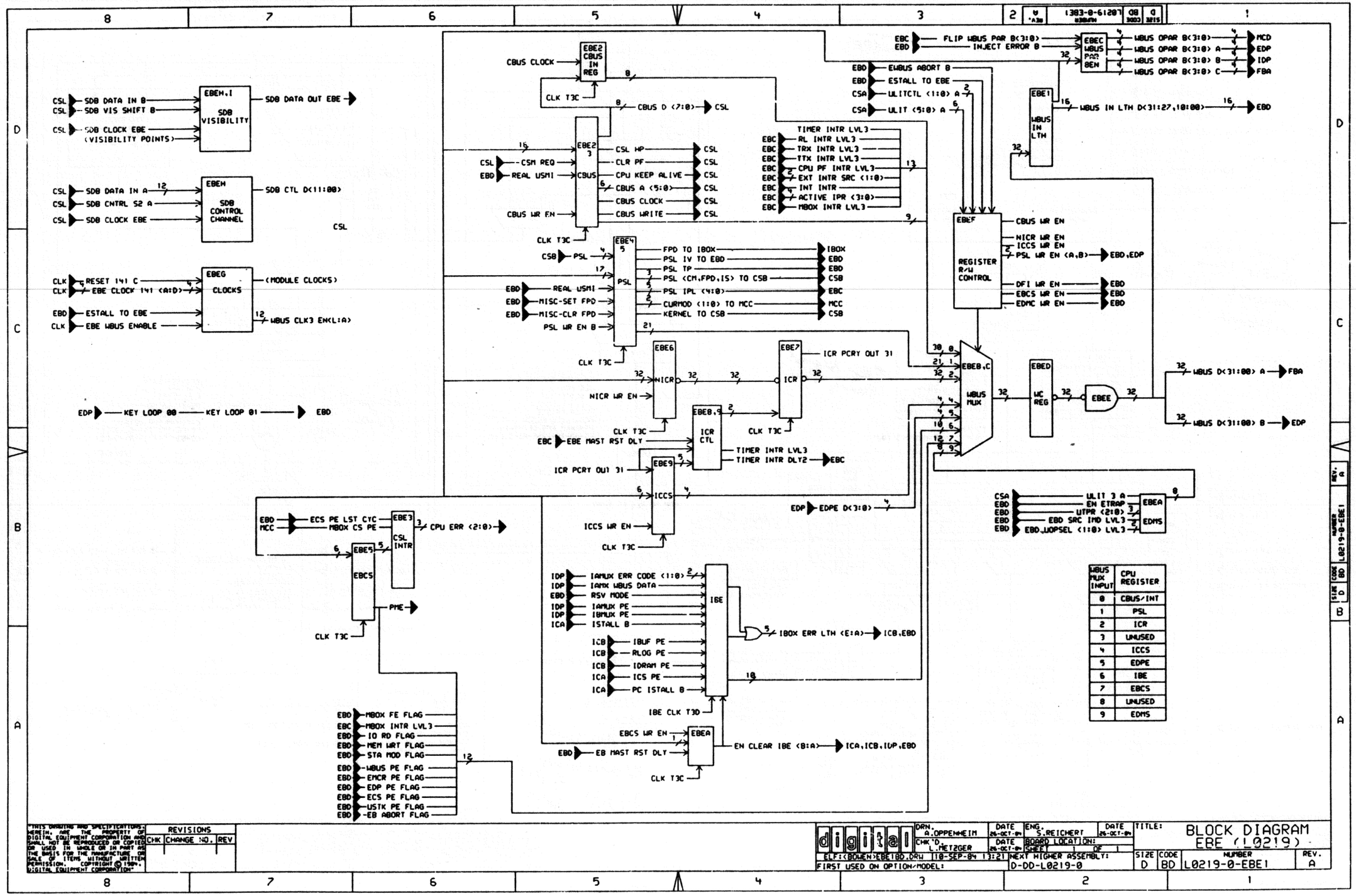
digital

DPN: C.CAIA221 — DATE 26-OCT-84
CHK'D: L.METZGER — DATE 26-OCT-84
ENG: M.EVANS — DATE 26-OCT-84
BOMPG LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY: D-DD-L0211-0
ELF1: COM1:EBD1BD.DPW 04-OCT-84 08:47
FIPST USED ON OPTION MODEL:

TITLE: EBD REGISTERS

SIZE	CODE	NUMBER	REV.
D	BD	L0211-0-EBD3	H

2232


EBEM.I
SDB VISIBILITY
SDB DATA IN B
SDB VIS SHIFT B
SDB CLOCK EBE (VISIBILITY POINTS)
SDB DATA OUT EBE
EBEM
SDB CONTROL CHANNEL
SDB DATA IN A
SDB CNTRL S2 A
SDB CLOCK EBE
SDB CTL D<11:00>
EBEG
CLOCKS
RESET 141 C
EBE CLOCK 141 <A:D>
ESTALL TO EBE
EBE WBUS ENABLE
<MODULE CLOCKS>
WBUS CLK3 EN<L:A>
EDP
KEY LOOP 00
KEY LOOP 01
EBD
EBE2 CBUS IN REG
CBUS CLOCK
CLK T3C
CBUS D <7:0>
EBE2 3 CBUS
CSM REQ
REAL USMI
CBUS WR EN
CSL WP
CLR PF
CPU KEEP ALIVE
CBUS A <5:0>
CBUS CLOCK
CBUS WRITE
TIMER INTR LVL3
RL INTR LVL3
TRX INTR LVL3
TTX INTR LVL3
CPU PF INTR LVL3
EXT INTR SRC <1:0>
INT INTR
ACTIVE IPR <3:0>
MBOX INTR LVL3
EBE4 5 PSL
CSB PSL
REAL USMI
MISC-SET FPD
MISC-CLR FPD
PSL WR EN B
FPD TO IBOX
PSL IV TO EBD
PSL TP
PSL <CM,FPD,IS> TO CSB
PSL IPL <4:0>
CURMOD <1:0> TO MCC
KERNEL TO CSB
IBOX
EBD
EBD
CSB
EBC
MCC
CSB
EBE6 NICR
NICR WR EN
EBE7 ICR
ICR PCRY OUT 31
EBE8,9 ICR CTL
EBC EBE MAST RST DLY
TIMER INTR LVL3
TIMER INTR DLY2
EBC
ICR PCRY OUT 31
EBE9 ICCS
ICCS WR EN
EDP EDPE D<3:0>
EBE3 CSL INTR
ECS PE LST CYC
MBOX CS PE
CPU ERR <2:0>
EBE5 EBCS
PME
MBOX FE FLAG
MBOX INTR LVL3
IO RD FLAG
MEM WRT FLAG
STA MOD FLAG
WBUS PE FLAG
EMCR PE FLAG
EDP PE FLAG
ECS PE FLAG
USTK PE FLAG
EB ABORT FLAG
IBE
IAMUX ERR CODE <1:0>
IAMX WBUS DATA
RSV MODE
IAMUX PE
IBMUX PE
ISTALL B
IBUF PE
RLOG PE
IDRAM PE
ICS PE
PC ISTALL B
IBE CLK T3D
IBOX ERR LTH <E:A>
ICB,EBD
EBEA
EBCS WR EN
EB MAST RST DLY
EN CLEAR IBE <B:A>
ICA,ICB,IDP,EBD
EBEC WBUS PAR GEN
FLIP WBUS PAR B<3:0>
INJECT ERROR B
WBUS OPAR B<3:0>
WBUS OPAR B<3:0> A
WBUS OPAR B<3:0> B
WBUS OPAR B<3:0> C
MCD
EDP
IDP
FBA
EBE1 WBUS IN LTH
WBUS IN LTH D<31:27,10:00>
EBD
EBD EWBUS ABORT B
EBD ESTALL TO EBE
CSA ULITCTL <1:0> A
CSA ULIT <5:0> A
EBEF REGISTER R/W CONTROL
CBUS WR EN
NICR WR EN
ICCS WR EN
PSL WR EN <A,B>
EBD,EDP
DFI WR EN
EBCS WR EN
EDMC WR EN
EBD
EBD
EBD
EBE8,C WBUS MUX
EBED WC REG
EBEE
WBUS D<31:00> A
FBA
WBUS D<31:00> B
EDP
CSA ULIT 3 A
EBD EM ETRAP
EBD UITPR <2:0>
EBD EBD SRC IMD LVL3
EBD EBD_UOPSEL <1:0> LVL3
EBEA EDMS
WBUS MUX INPUT
CPU REGISTER
0 CBUS/INT
1 PSL
2 ICR
3 UNUSED
4 ICCS
5 EDPE
6 IBE
7 EBCS
8 UNUSED
9 EDMS
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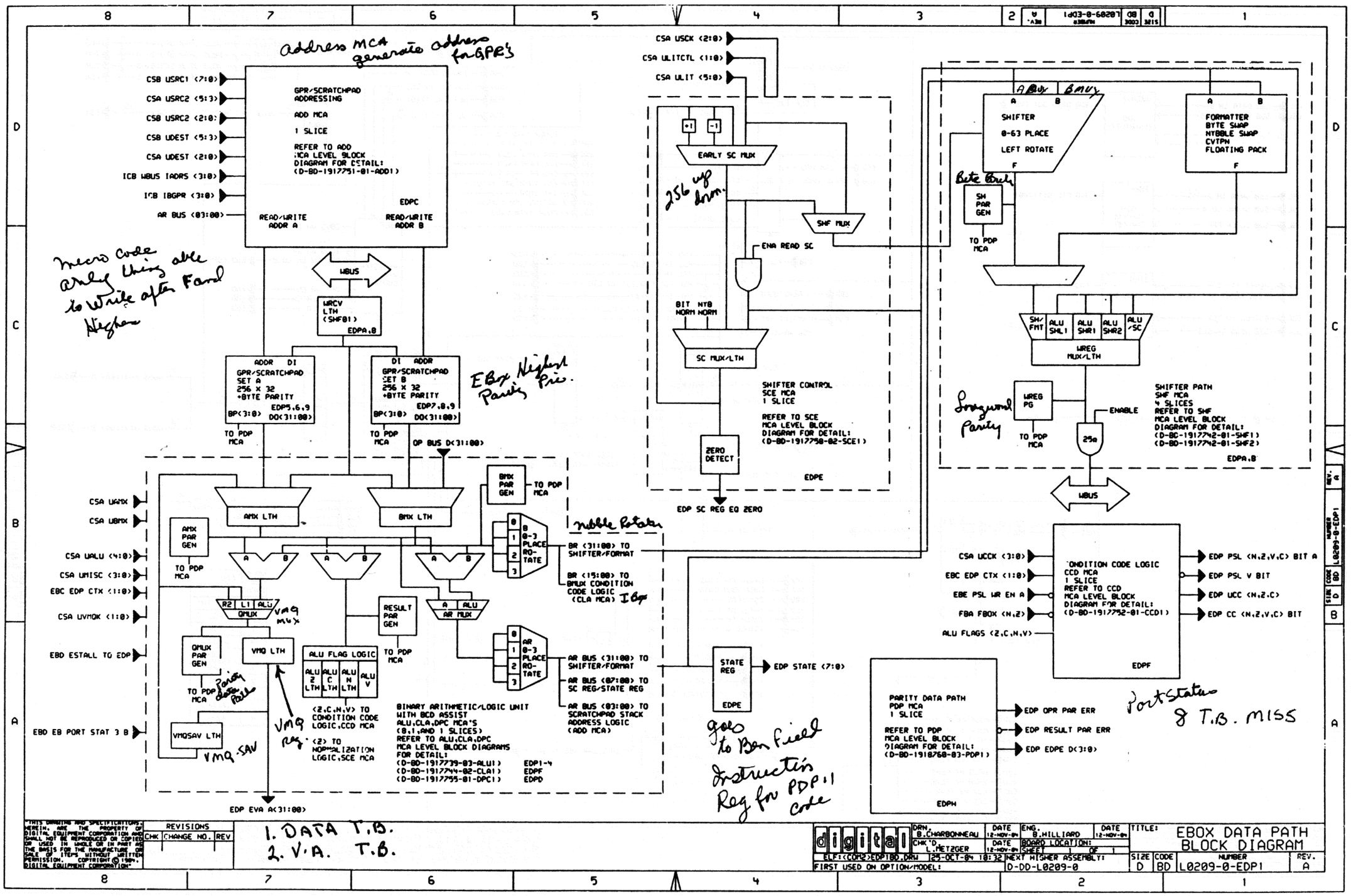
REVISIONS
CHK
CHANGE NO.
REV
digital
DRN. A.OPPENHEIM
CHK'D. L.METZGER
ENG. S.REICHERT
DATE 26-OCT-84
BOARD LOCATION:
SHEET 1 OF
ELF:<BOWEN>EBE1BD.DRW 18-SEP-84 13:21
FIRST USED ON OPTION/MODEL:
NEXT HIGHER ASSEMBLY: D-DD-L0219-0
TITLE: BLOCK DIAGRAM EBE (L0219)
SIZE D
CODE BD
NUMBER L0219-0-EBE1
REV. A


Address MCA generate address for GPR's
CSB USRC1 <7:0>
CSA USRC2 <5:3>
CSB USRC2 <2:0>
CSB UDEST <5:3>
CSA UDEST <2:0>
ICB WBUS IADRS <3:0>
ICB IBGPR <3:0>
AR BUS <03:00>
GPR/SCRATCHPAD ADDRESSING
ADD MCA
1 SLICE
REFER TO ADD MCA LEVEL BLOCK DIAGRAM FOR DETAIL: (D-BD-1917751-01-ADD1)
EDPC
READ/WRITE ADDR A
READ/WRITE ADDR B
Micro code only thing able to Write after Fand Higher
WBUS
WRCV LTH (SHF01)
EDPA.8
ADDR DI GPR/SCRATCHPAD SET A 256 x 32 +BYTE PARITY
EDP5,6,9
BP(3:0) DO(31:00)
DI ADDR GPR/SCRATCHPAD SET B 256 x 32 +BYTE PARITY
EDP7,8,9
BP(3:0) DO(31:00)
EBox Highest Priority
TO PDP MCA
OP BUS D<31:00>
BMX PAR GEN
TO PDP MCA
CSA UAMX
CSA UBMX
AMX LTH
BMX LTH
AMX PAR GEN
TO PDP MCA
CSA UALU <4:0>
CSA UMISC <3:0>
EBC EDP CTX <1:0>
CSA UVMOK <1:0>
EBD ESTALL TO EDP
EBD EB PORT STAT 3 B
A B
R2 L1 ALU QMUX
VMQ MUX
QMUX PAR GEN
TO PDP MCA
Parity data path
VMQ LTH
VMQSAV LTH
VMQ.SAV
VMQ Reg
ALU FLAG LOGIC
ALU Z LTH
ALU C LTH
ALU N LTH
ALU V
<Z,C,N,V> TO CONDITION CODE LOGIC,CCD MCA
<Z> TO NORMALIZATION LOGIC,SCE MCA
RESULT PAR GEN
TO PDP MCA
A ALU
AR MUX
0 B 0-3 PLACE ROTATE
BR <31:00> TO SHIFTER/FORMAT
BR <15:00> TO BMUX CONDITION CODE LOGIC (CLA MCA) IOp
0 AR 0-3 PLACE ROTATE
AR BUS <31:00> TO SHIFTER/FORMAT
AR BUS <07:00> TO SC REG/STATE REG
AR BUS <03:00> TO SCRATCHPAD STACK ADDRESS LOGIC (ADD MCA)
BINARY ARITHMETIC/LOGIC UNIT WITH BCD ASSIST ALU,CLA,DPC MCA'S (8,1,AND 1 SLICES) REFER TO ALU,CLA,DPC MCA LEVEL BLOCK DIAGRAMS FOR DETAIL: (D-BD-1917739-03-ALU1) EDP1-4 (D-BD-1917744-02-CLA1) EDPF (D-BD-1917755-01-DPC1) EDPD
Nibble Rotate
EDP EVA A<31:00>
CSA USCK <2:0>
CSA ULITCTL <1:0>
CSA ULIT <5:0>
+1
-1
EARLY SC MUX
256 up down
SHF MUX
ENA READ SC
BIT NYB NORM NORM
SC MUX/LTH
SHIFTER CONTROL SCE MCA 1 SLICE
REFER TO SCE MCA LEVEL BLOCK DIAGRAM FOR DETAIL: (D-BD-1917758-02-SCE1)
ZERO DETECT
EDPE
EDP SC REG EQ ZERO
A BUS B BUS
A B
SHIFTER 0-63 PLACE LEFT ROTATE
F
A B
FORMATTER BYTE SWAP NYBBLE SWAP CVTPN FLOATING PACK
F
Byte Parity
SH PAR GEN
TO PDP MCA
SH/FMT ALU SML1 ALU SHR1 ALU SHR2 ALU /SC
WREG MUX/LTH
Longword Parity
WREG PG
TO PDP MCA
ENABLE
25a
SHIFTER PATH SHF MCA 4 SLICES REFER TO SHF MCA LEVEL BLOCK DIAGRAM FOR DETAIL: (D-BC-1917742-01-SHF1) (D-BD-1917742-01-SHF2)
EDPA.8
WBUS
CSA UCCK <3:0>
EBC EDP CTX <1:0>
EBE PSL WR EN A
FBA FBOX <N,Z>
ALU FLAGS <Z,C,N,V>
CONDITION CODE LOGIC CCD MCA 1 SLICE REFER TO CCD MCA LEVEL BLOCK DIAGRAM FOR DETAIL: (D-BD-1917752-01-CCD1)
EDPF
EDP PSL <N,Z,V,C> BIT A
EDP PSL V BIT
EDP UCC <N,Z,C>
EDP CC <N,Z,V,C> BIT
Port Status
8 T.B. MISS
STATE REG
EDPE
EDP STATE <7:0>
goes to Bon Field Instructin Reg for PDP-11 code
PARITY DATA PATH PDP MCA 1 SLICE
REFER TO PDP MCA LEVEL BLOCK DIAGRAM FOR DETAIL: (D-BD-1918768-03-PDP1)
EDPH
EDP OPR PAR ERR
EDP RESULT PAR ERR
EDP EDPE D<3:0>
1. DATA T.B.
2. V.A. T.B.
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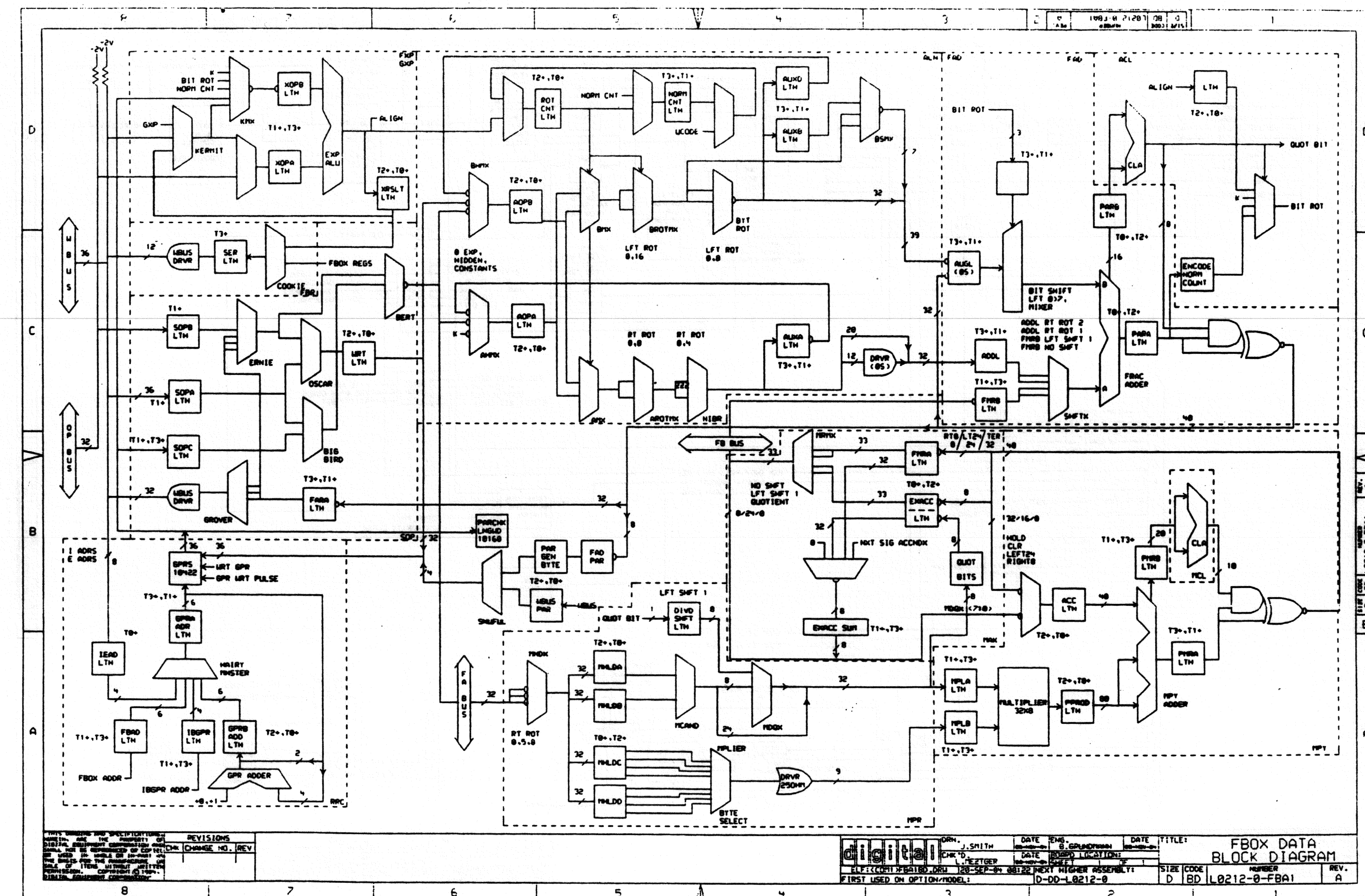
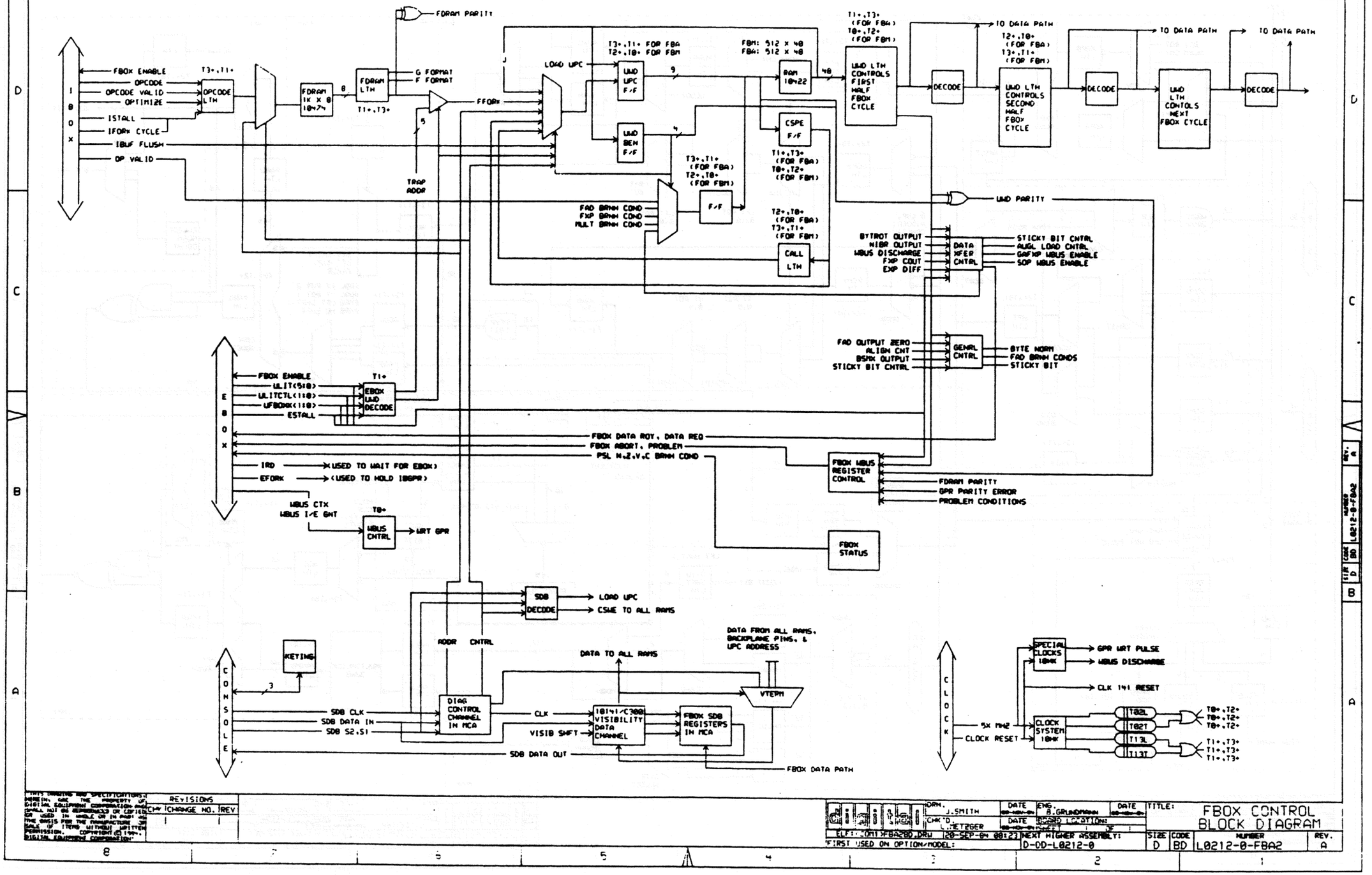
REVISIONS
CHK CHANGE NO. REV
digital
DRN. B.CHARBONNEAU DATE 12-NOV-84
CHK'D L.METZGER DATE 12-NOV-84
ENG. B.WILLIARD DATE 12-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF1<COM2>EDPTBD.DAV 25-OCT-84 10:32
NEXT HIGHER ASSEMBLY: D-DD-L0209-0
FIRST USED ON OPTION/MODEL:
TITLE: EBOX DATA PATH BLOCK DIAGRAM
SIZE D CODE BD NUMBER L0209-0-EDP1 REV. A


FBOX DATA
BLOCK DIAGRAM
digital
J.SMITH
L.METZGER
B.GRUNDMANN
ELF:(COM1)FBA1BD.DRW
FIRST USED ON OPTION/MODEL:
D-DD-L0212-0
SIZE
D
CODE
BD
NUMBER
L0212-0-FBA1
REV.
A
REVISIONS
CHANGE NO.
W BUS
OP BUS
FA BUS
FB BUS
EXP ALU
XOPB LTH
XOPA LTH
XRSLT LTH
KERMIT
ALIGN
GXP
BIT ROT
NORM CNT
SER LTH
WBUS DRVR
FBOX REGS
COOKIE
BERT
SOPB LTH
SOPA LTH
SOPC LTH
ERNIE
OSCAR
BIG BIRD
URT LTH
GROVER
FARA LTH
GPRS 16X22
URT GPR
GPR URT PULSE
GPRA ADR LTH
HAIRY MONSTER
IEAD LTH
FBAD LTH
IBGPR LTH
GPRB ADD LTH
GPR ADDER
FBOX ADDR
IBGPR ADDR
RPC
BMRX
AOPB LTH
AOPA LTH
AMRX
BMX
BROTMX
BIT ROT
LFT ROT 0,16
LFT ROT 0,8
RT ROT 0,8
RT ROT 0,4
AMX
AROTMX
NIBR
ROT CNT LTH
NORM CNT LTH
UCODE
AUXD LTH
AUXB LTH
AUXA LTH
BSMX
DRVR (05)
AUGL (05)
BIT SHIFT LFT 0>7, MIXER
ADDL
FMRB LTH
SHFTX
FRAC ADDER
PARA LTH
PARB LTH
CLA
QUOT BIT
ENCODE NORM COUNT
PARCHK LMGUD 10160
PAR GEN BYTE
FAD PAR
SHUFUL
WBUS PAR
DIVD SHFT LTH
LFT SHFT 1
FMRA LTH
EXACC LTH
NXT SIG ACCNDX
EXACC SUM
QUOT BITS
ACC LTH
FMRB LTH
MCL
NO SHFT LFT SHFT 1 QUOTIENT
MMDX
MMLDA
MMLDB
MMLDC
MMLDD
MCAND
MDOX
MPLIER
BYTE SELECT
DRVR 250MM
MPLA LTH
MPLB LTH
MULTIPLIER 32X8
PPROD LTH
MPY ADDER
FMRA LTH
RT ROT 0,5,8
8 EXP, HIDDEN, CONSTANTS
MPR
MPY

2235



REVISIONS		
CHAR	CHANGE NO.	REV
1	1	

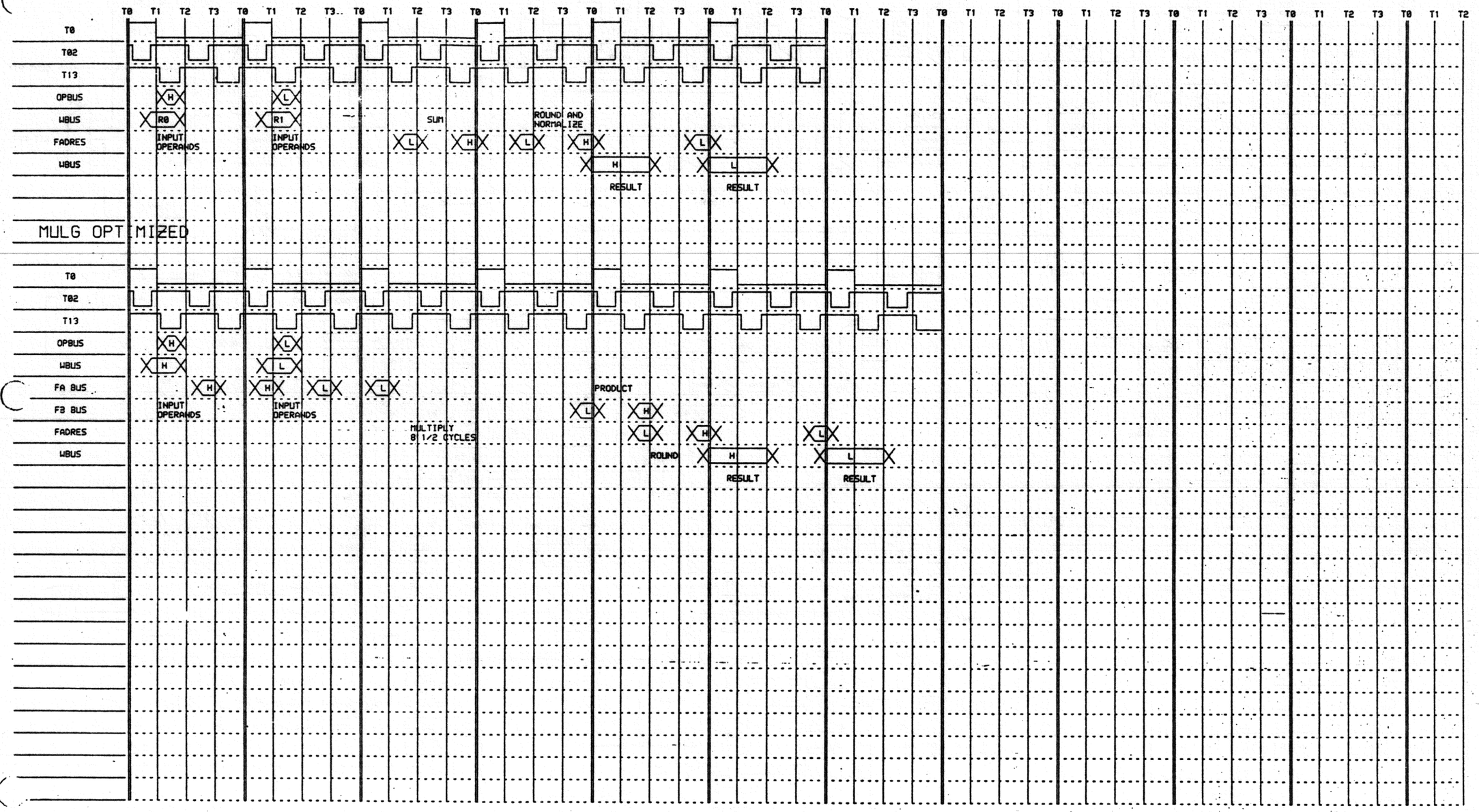
DRN. J.SMITH	DATE	ENG. B.GRUNDMANN	DATE
CHK'D L.METZGER	DATE	BOARD LOCATION:	
ELF: CONT>FBA2BD.DRW 20-SEP-84 08:23		NEXT HIGHER ASSEMBLY: D-DD-L0212-0	
FIRST USED ON OPTION/MODEL:			

TITLE: FBOX CONTROL BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0212-0-FBA2	A

2236

ADDG OPTIMIZED

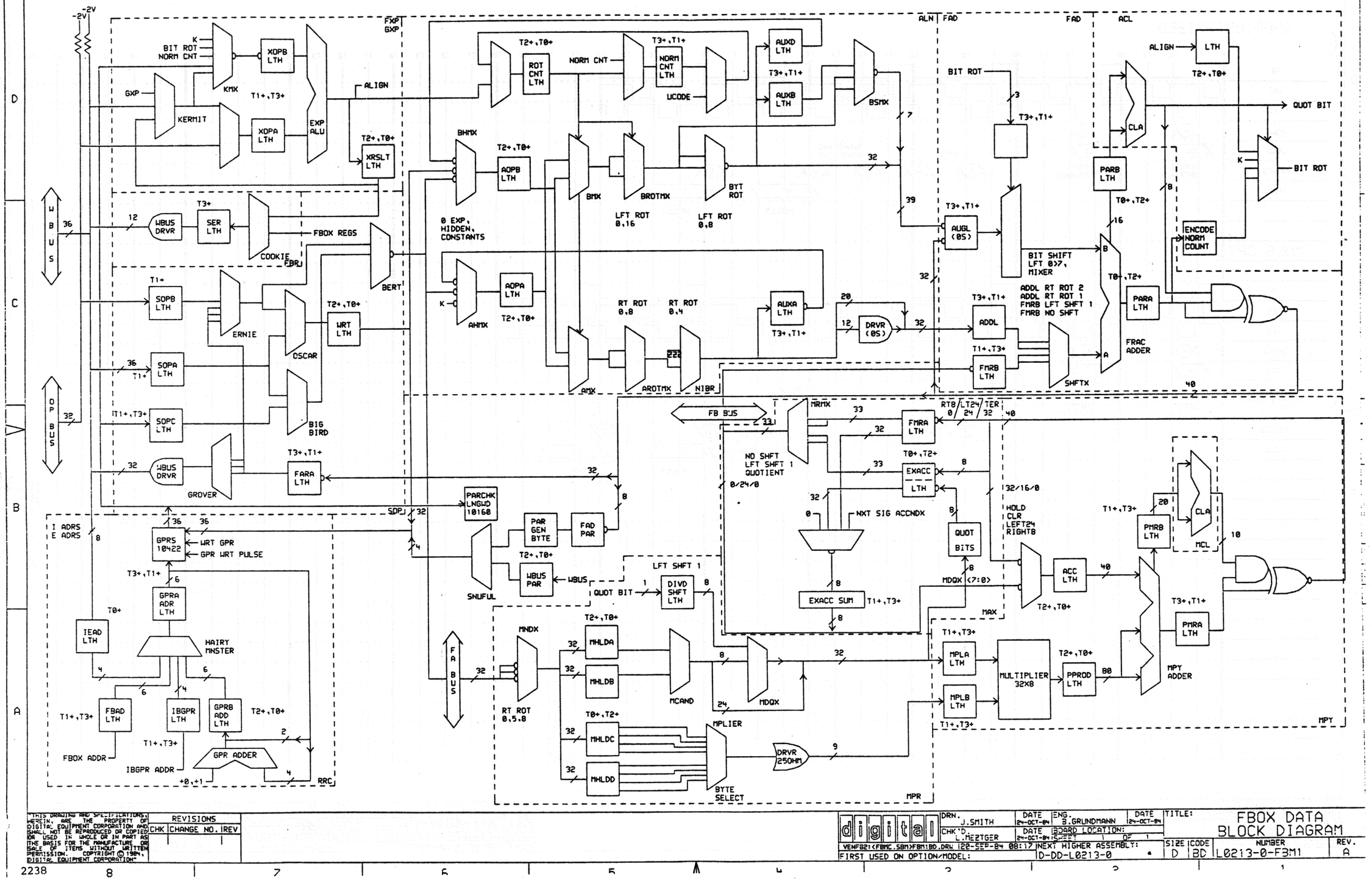


MULG OPTIMIZED

REVISIONS		
CHK	CHANGE NO.	REV

digital

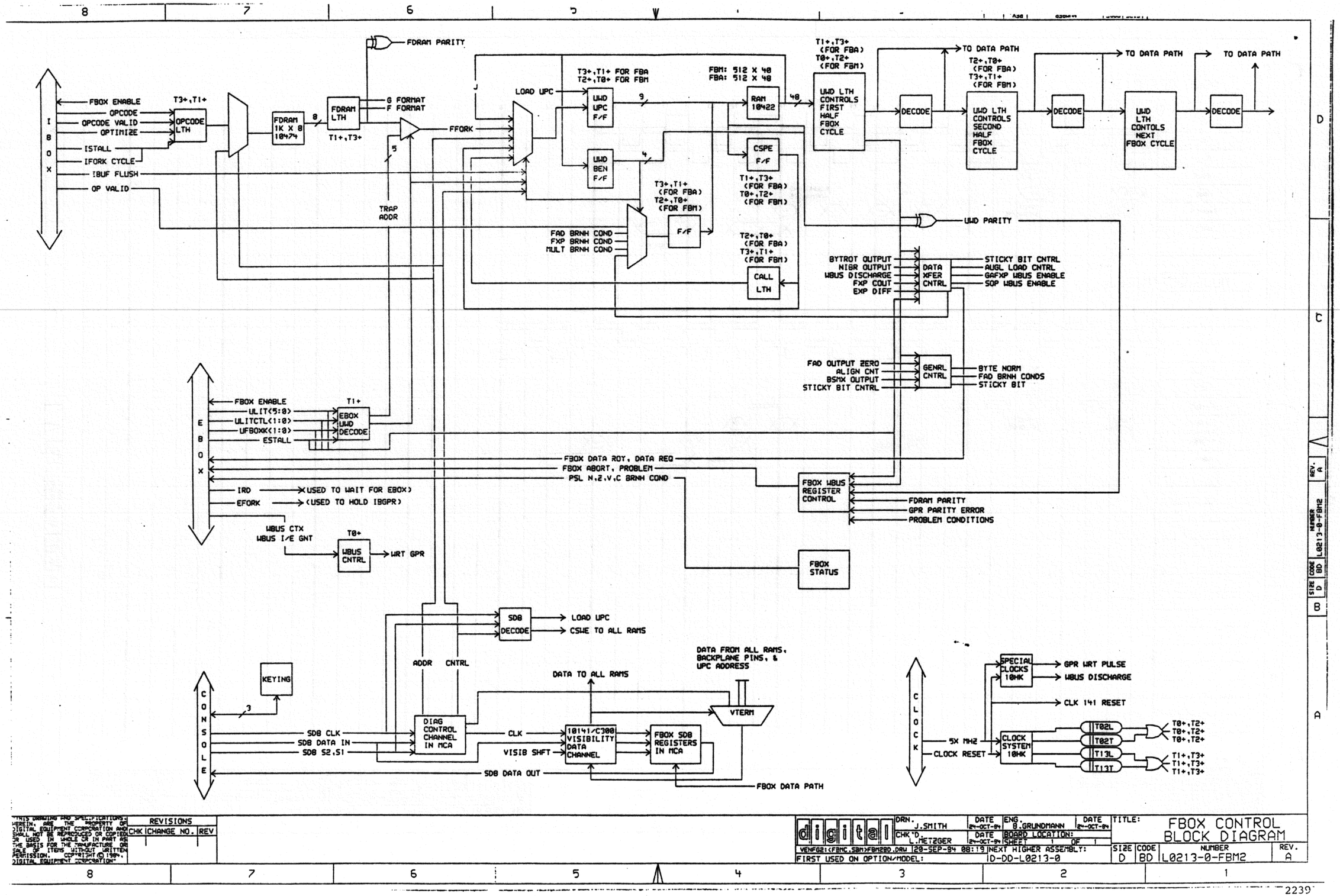
DRN. C.CAIAZZI	DATE 21-SEP-84	ENG. B.GRUNDMANN	DATE 21-SEP-84	TITLE: FBOX TIMING DIAGRAM	
CHK'D L.METZGER	DATE 21-SEP-84	BOARD LOCATION: SHEET 1 OF 1			
VENFG21:<FBME.SRC>FBOX-TIMING.DAV;20	20-SEP-84 08:25	NEXT HIGHER ASSEMBLY:		SIZE D / CODE TD / NUMBER L0212-0-FBA1 / REV. A	
FIRST USED ON OPTION/MODEL:		D-DD-L0212-0			



REVISIONS		
CHK	CHANGE NO.	REV

digital	DRN. J.SMITH	DATE 24-OCT-84	ENG. B.GRUNDMANN	DATE 24-OCT-84	TITLE:	FBOX DATA BLOCK DIAGRAM
	CHK'D L.MEZTGER	DATE 24-OCT-84	BOARD LOCATION: SHEET 1 OF 1			
VENFB2:<FBMC.SBM>FBM1BD.DRW 20-SEP-84 08:17			NEXT HIGHER ASSEMBLY: D-DD-L0213-0 A		SIZE D / CODE BD / NUMBER L0213-0-F3M1	REV. A
FIRST USED ON OPTION/MODEL:						

2238



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. J.SMITH	DATE 24-OCT-84	ENG. B.GRUNDMANN	DATE 24-OCT-84
CHK D. L.METZGER	DATE 24-OCT-84	BOARD LOCATION: SHEET 1 OF 1	

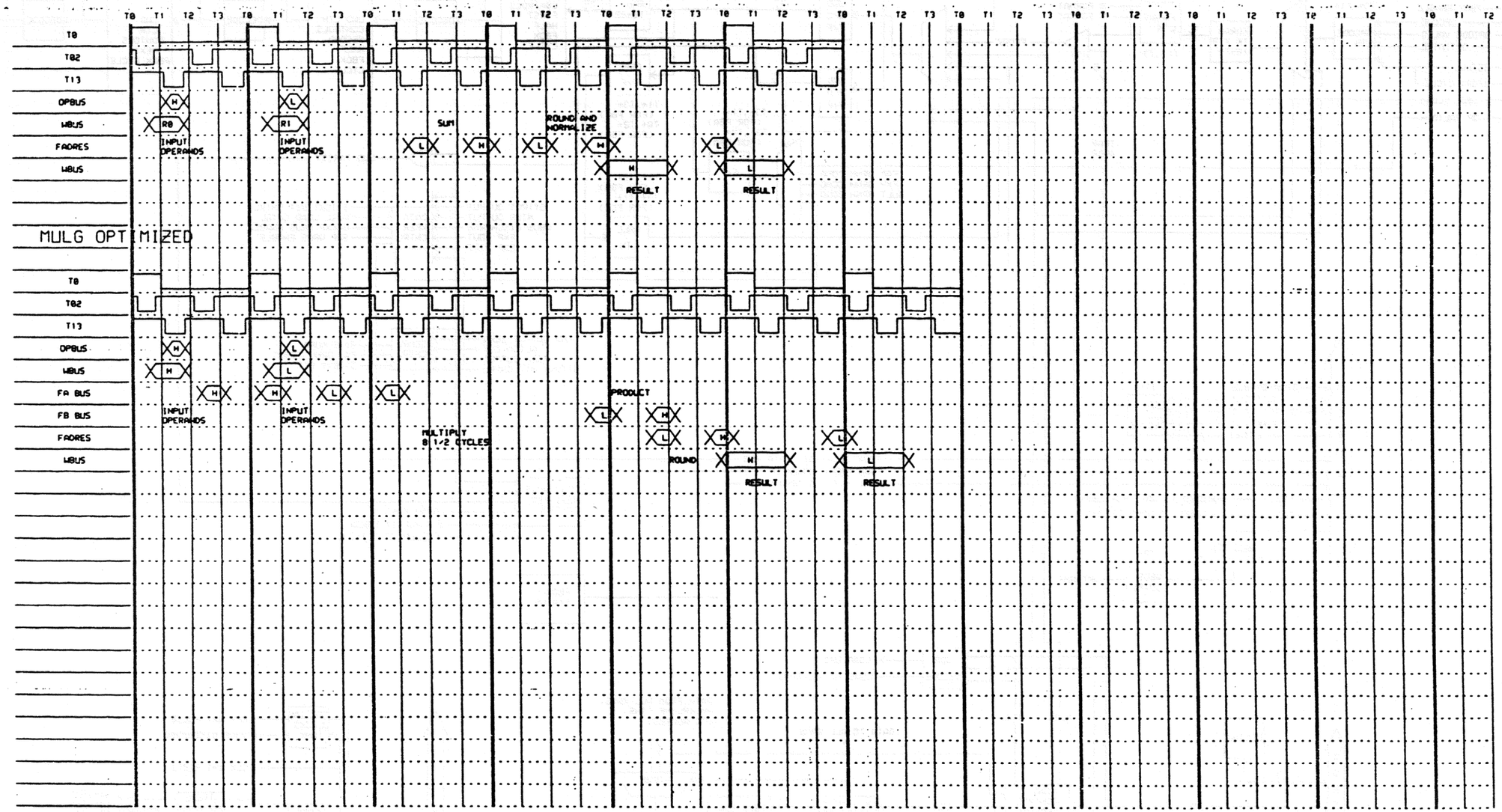
VENFG2::FBMC.SBM>FBM2BD.DRW 20-SEP-84 08:19 | NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL: | D-DD-L0213-0

TITLE: FBOX CONTROL BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0213-0-FBM2	A

2239

ADDG OPTIMIZED



MULG OPTIMIZED

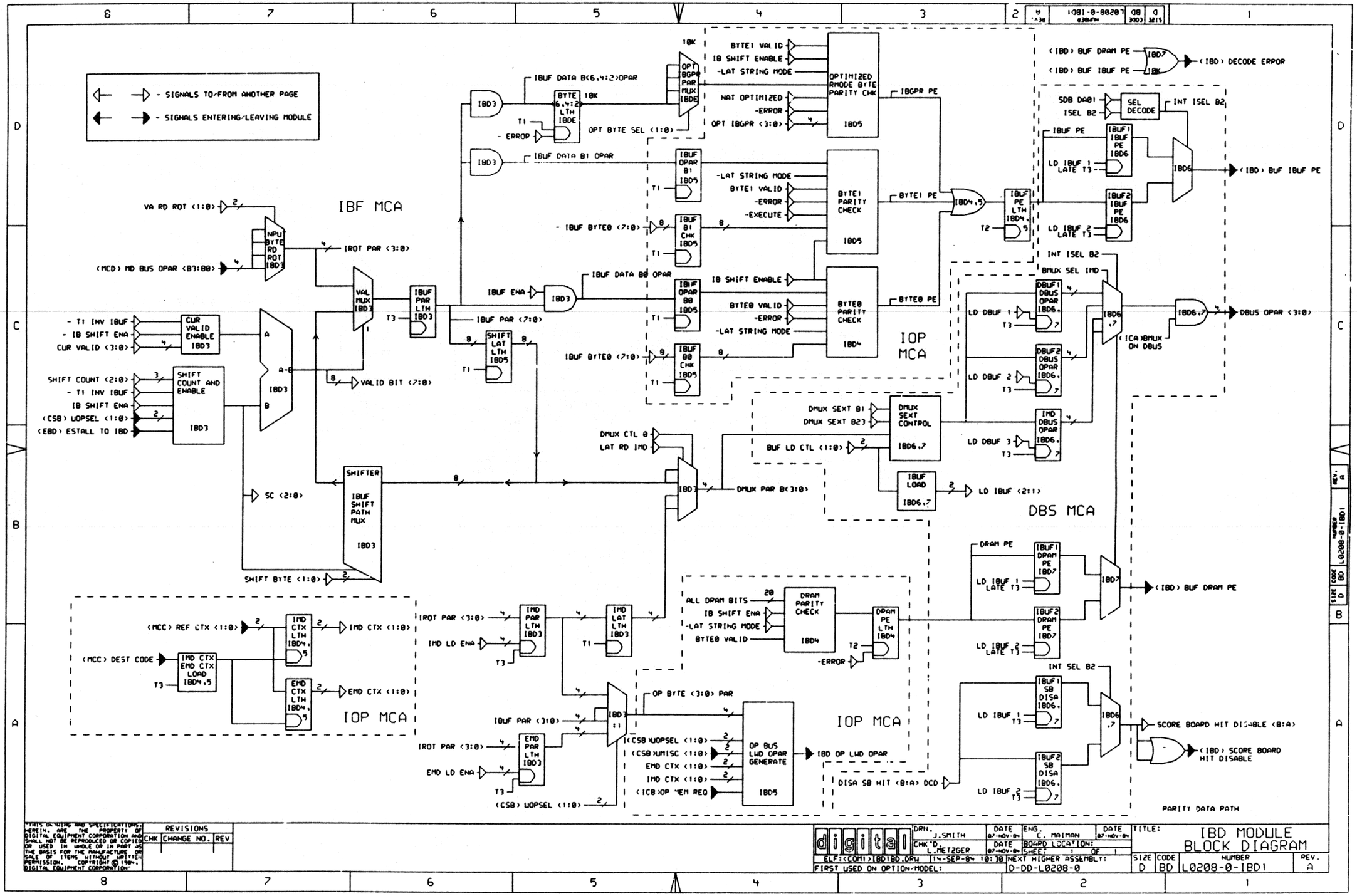
REVISIONS		
CHK	CHANGE NO.	REV

DRN: C.CAIAZZI — DATE: 25-OCT-84
CHK'D: L.METZGER — DATE: 25-OCT-84
ENG: R.GRUNDMANN — DATE: 25-OCT-84
SCALE: — LOCATION: — SHT: 1 OF 1
ELF:(COMIX)FBM1TO.DRW 26-SEP-84 13:49
FIRST USED ON OPTION-MODEL:
NEXT HIGHER ASSEMBLY: D-DD-L0213-0

TITLE: FBOX TIMING DIAGRAM

SIZE	CODE	NUMBER	REV.
D	TD	L0213-0-FBM1	A

2240

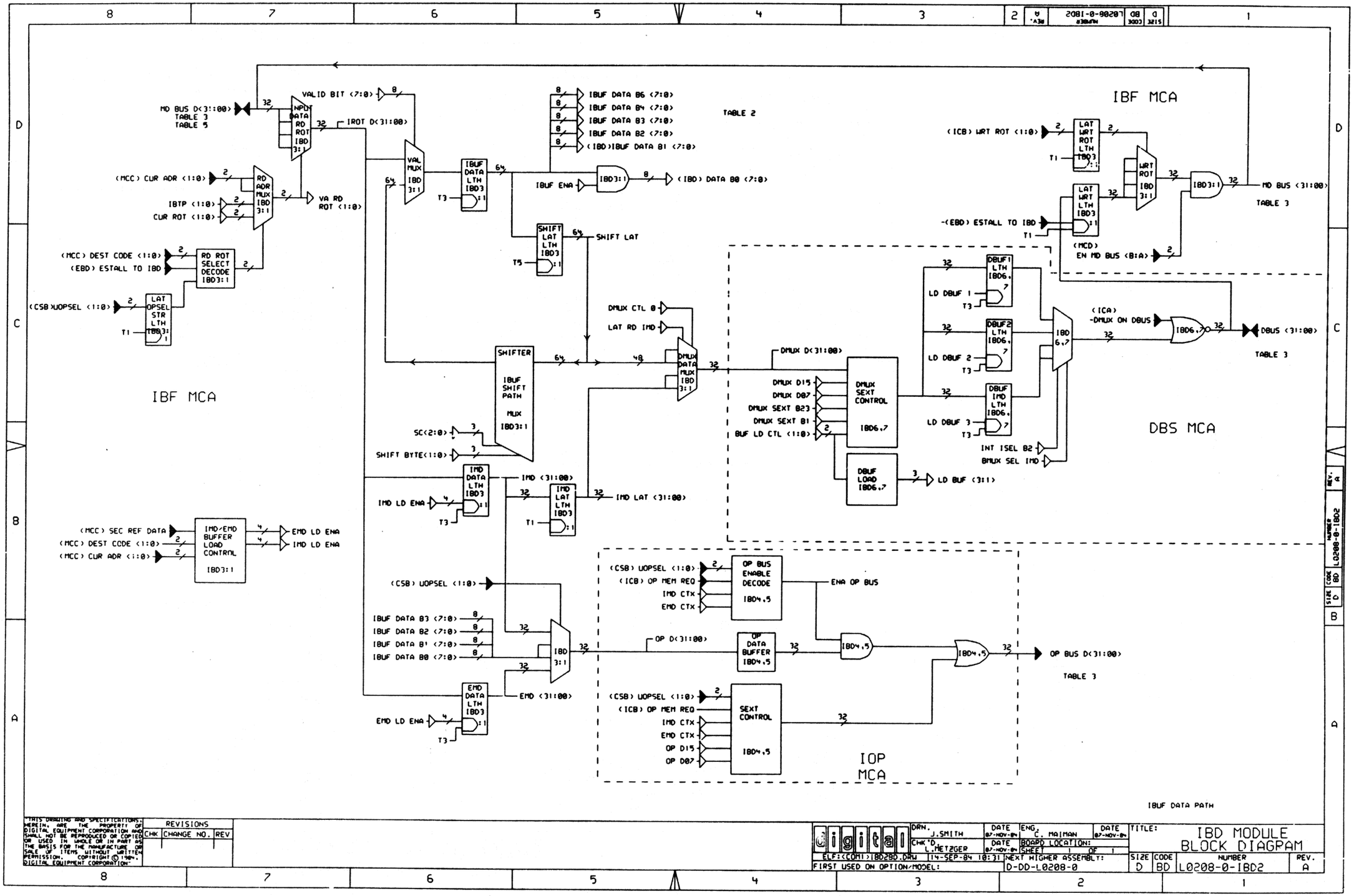


DRN. J.SMITH	DATE 07-NOV-84	ENG. C. MAIMAN	DATE 07-NOV-84	TITLE: IBD MODULE BLOCK DIAGRAM			
CHK'D L.METZGER	DATE 07-NOV-84	BOARD LOCATION:					
ELF:<COM1>IBD1BD.DRW 14-SEP-84 10:30		NEXT HIGHER ASSEMBLY:		SIZE D	CODE BD	NUMBER L0208-0-IBD1	REV. A
FIRST USED ON OPTION/MODEL:		D-DD-L0208-0		SHEET 1 OF 1			

REVISIONS

CHK	CHANGE NO.	REV

2241



REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. J.SMITH — DATE 07-NOV-84
CHK'D L.METZGER — DATE 07-NOV-84
ENG. C. MAIMAN — DATE 07-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:<COM1>IBD2BD.DRW 14-SEP-84 10:31
NEXT HIGHER ASSEMBLY: D-DD-L0208-0
FIRST USED ON OPTION/MODEL:

TITLE: IBD MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0208-0-IBD2	A

2242

IBD4
IBD8

VALID CNT DECODE 10K

BYTE 1 VALID
BYTE 0 VALID
VALID CODE SPD <2:0>

BYTE1 R=PC DECODE 10K

B1 REG IS PC

IBUF BYTE1 <7:4>

T1 INV IBUF
(ICA) STRING MODE
PREV BDEST NEXT
EPC EQL 0
FD FLAG
IB SHIFT ENA
(CSA) UMISC <1:0> B
IBUF BYTE0 <7:0>
IBUF BYTE1 <7:4>
NAT LAST
NAT CTX <2:0>
NAT CTL <1:0>

SPD MCA
:IBD9

SPECIFER DECODE

IBD9

DMUX SEXT B1
DMUX SEXT B23
DMUX CTL 0

DELTA PC <2:0>

IB STATE

SHIFT BYTE <1:0> (B:A)
SHIFT COUNT <2:0> (B:A)

NAT OPTIMIZED
OPT BYTE SEL <1:0>

UNLAT CUR VALID <3:0>

10K

CUR VALID <3:0>

-ERROR T1

(DISABLE OPTIMIZATIONS) SDB DA02

IBUF DATA B6 <7:4>
IBUF DATA B4 <7:4>
IBUF DATA B3 <7:4>
IBUF DATA B2 <7:0>

RMODE FINDER 10K IBD9

IBUF B<6,4,3,2> RMODE

IBUF BYTE0 <7:0> G

BYTE0 LAT LTH IBDE

LAT BYTE0 <7:0>

IBUF DATA B1 <7:0>

10K IBD3:1

IBUF BYTE1 <7:0> (C:A)

-LAT CTL <1:0>

10K DRAM EXECUTE DECODE IBD5

EXECUTE

IBUF DATA B6 <3:0>
IBUF DATA B4 <3:0>
IBUF DATA B3 <3:0>
IBUF DATA B2 <3:0>

IBUF B6 <3:0> IBDE
IBUF B4 <3:0> IBDE
IBUF B3 <3:0> IBDE
IBUF B1 <3:0> IBDE

-ERROR T1

IBDE

OPT IBGPR <3:0>

LAT BYTE1 <3:0>

SEL IBGPR <3:0>

NAT OPTIMIZE

TABLE 1

INT PC SEL B2

IBUF1 DELTA PC LTH IBD6
IBUF2 DELTA PC LTH IBD6

LD IBUF 1 T3
LD IBUF 2 T3

IBD6

<IBD> BUF DELTA PC <2:0>

IBUF1 OPT LTH IBD6
IBUF2 OPT LTH IBD6

-<IBD> OPTIMIZED

PC SEL B2

IBUF1 IBGPR LTH IBD7
IBUF2 IBGPR LTH IBD7

IBD7

<IBD> IBGPR <3:0>

IBUF1 IGPR LTH IBD7
IBUF2 IGPR LTH IBD7

<IBD> IGPR <3:0>

DBS MCA

IBUF BYTE1 <3:0>

BYTE LAT LTH IBDE

VT LAT BYTE1 <3:0>

SDB DA01

INT PC SEL B2

PC SEL B2

SDB LD A<07:00>
IBUF DATA B0 <7:0>
FD FLAG
SBD LD A11
EPC BIT <2:0>
SDB LD A<10:08>

10K IBD3:1
10K IBDD
10K IBD8

SDB DA <09:00>

IBUF BYT0 <7:0> (G:A)

BUF FD FLAG (C:A)

BUF EPC <2:0> (C:A)

WR LOW DRAM
WR HIGH DRAM

10K NATIVE MODE DRAM 4K x 20 IBDB IBDC

D A W W DO

20

VT NAT CTX <2:0>
VT NAT TYPE <1:0>
VT NAT REF <1:0>
VT NAT CTL <1:0>
VT NAT SUSPEND
VT NAT BDEST NEXT
VT NAT LAST
VT NAT OPAR
VT NAT FPA
VT NAT ADRS <5:0>

DRAM DATA ERR LTH IBDD

-ERROR T1

20

VT LAT CTX <2:0>
VT LAT TYPE <1:0>
VT LAT REF <1:0>
VT LAT CTL <1:0>
VT LAT SUSPEND
VT LAT BDEST NEXT
VT LAT LAST
VT LAT OPAR
VT LAT FPA
VT LAT ADRS <5:0>

TO DRAM PARITY CHECK
(ALL DRAM BITS)

SPECIFIER DECODE AND DRAM

REVISIONS

CHK	CHANGE NO.	REV

DRN T. KNIGHT	DATE 07-NOV-84	ENG. C. MAIMAN	DATE 07-NOV-84
CHK D. L.METZGER	DATE 07-NOV-84	BOARD LOCATION: SHEET 1 OF 1	

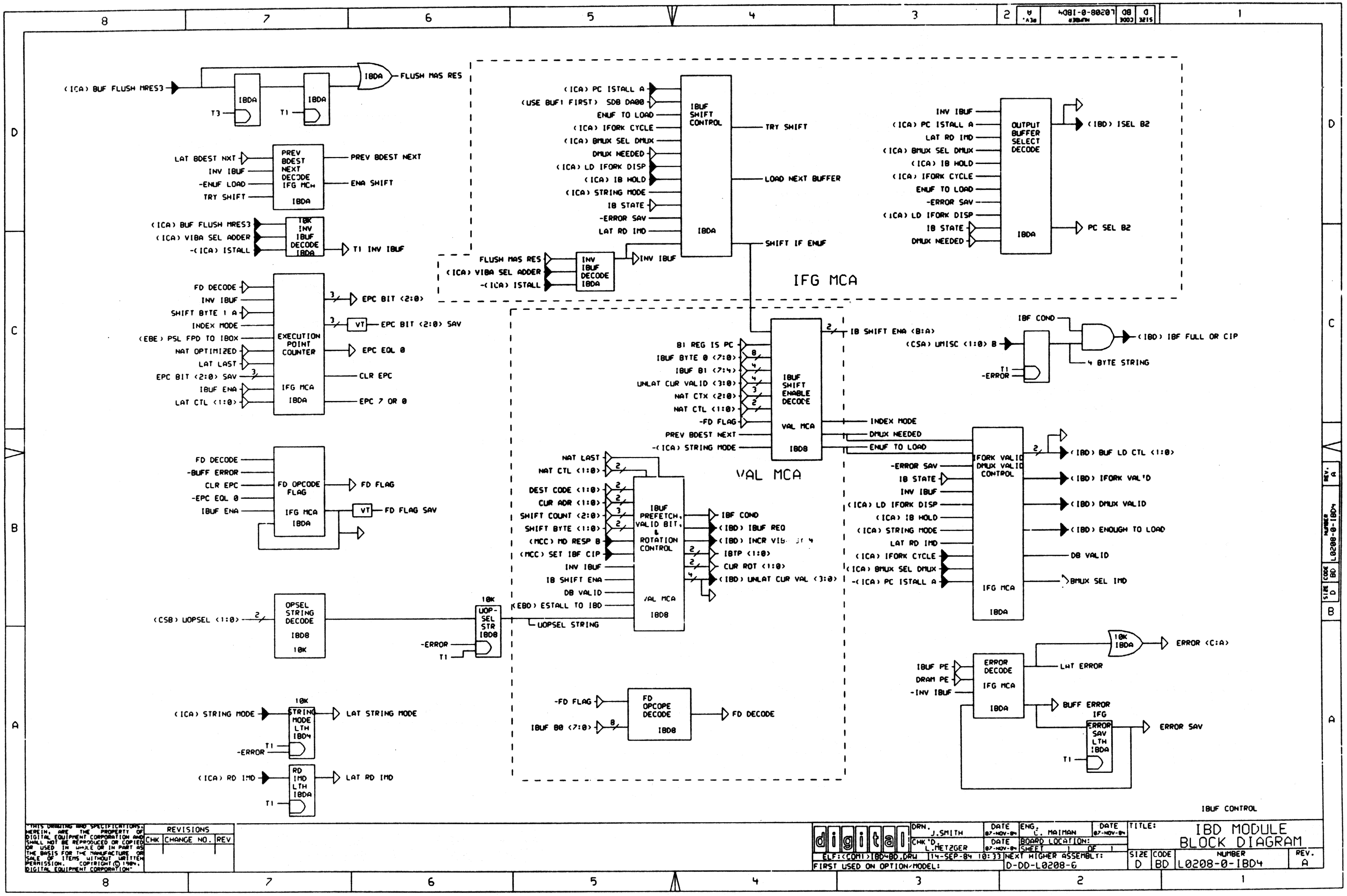
ELF:<COMI>IBDBD.DRW 14-SEP-84 10:32 NEXT HIGHER ASSEMBLY: D-DD-L0208-0

FIRST USED ON OPTION MODEL:

TITLE: IBD MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0208-0-IBD3	A

2243


(ICA) BUF FLUSH MRES3
IBDA
T3
T1
FLUSH MAS RES
LAT BDEST NXT
INV IBUF
-ENUF LOAD
TRY SHIFT
PREV BDEST NEXT DECODE IFG MCA IBDA
PREV BDEST NEXT
ENA SHIFT
(ICA) BUF FLUSH MRES3
(ICA) VIBA SEL ADDER
-(ICA) ISTALL
10K INV IBUF DECODE IBDA
T1 INV IBUF
FD DECODE
SHIFT BYTE 1 A
INDEX MODE
(EBE) PSL FPD TO IBOX
NAT OPTIMIZED
LAT LAST
EPC BIT (2:0) SAV
IBUF ENA
LAT CTL (1:0)
EXECUTION POINT COUNTER
IFG MCA
EPC BIT (2:0)
VT
EPC BIT (2:0) SAV
EPC EQL 0
CLR EPC
EPC 7 OR 0
-BUFF ERROR
CLR EPC
-EPC EQL 0
FD OPCODE FLAG
FD FLAG
FD FLAG SAV
(CSB) UOPSEL (1:0)
OPSEL STRING DECODE IBD8 10K
-ERROR
10K UOP-SEL STR IBD8
(ICA) STRING MODE
10K STRING MODE LTH IBD4
LAT STRING MODE
(ICA) RD IMD
RD IMD LTH IBDA
LAT RD IMD
(ICA) PC ISTALL A
(USE BUF1 FIRST) SDB DA00
ENUF TO LOAD
(ICA) IFORK CYCLE
(ICA) BMUX SEL DMUX
DMUX NEEDED
(ICA) LD IFORK DISP
(ICA) IB HOLD
(ICA) STRING MODE
IB STATE
-ERROR SAV
IBUF SHIFT CONTROL
TRY SHIFT
LOAD NEXT BUFFER
SHIFT IF ENUF
FLUSH MAS RES
(ICA) VIBA SEL ADDER
-(ICA) ISTALL
INV IBUF DECODE IBDA
INV IBUF
IFG MCA
OUTPUT BUFFER SELECT DECODE
(IBD) ISEL B2
PC SEL B2
B1 REG IS PC
IBUF BYTE 0 (7:0)
IBUF B1 (7:4)
UNLAT CUR VALID (3:0)
NAT CTX (2:0)
NAT CTL (1:0)
-FD FLAG
PREV BDEST NEXT
-(ICA) STRING MODE
IBUF SHIFT ENABLE DECODE
VAL MCA
IBD8
IB SHIFT ENA (B:A)
(CSA) UMISC (1:0) B
IBF COND
(IBD) IBF FULL OR CIP
4 BYTE STRING
NAT LAST
DEST CODE (1:0)
CUR ADR (1:0)
SHIFT COUNT (2:0)
SHIFT BYTE (1:0)
(MCC) MD RESP B
(MCC) SET IBF CIP
IB SHIFT ENA
DB VALID
(EBD) ESTALL TO IBD
UOPSEL STRING
IBUF PREFETCH, VALID BIT, & ROTATION CONTROL
(IBD) IBUF REQ
IBTP (1:0)
CUR ROT (1:0)
(IBD) UNLAT CUR VAL (3:0)
INDEX MODE
DMUX NEEDED
ENUF TO LOAD
IFORK VALID DMUX VALID CONTROL
(IBD) BUF LD CTL (1:0)
(IBD) IFORK VAL'D
(IBD) DMUX VALID
(IBD) ENOUGH TO LOAD
DB VALID
BMUX SEL IMD
-(ICA) PC ISTALL A
-FD FLAG
IBUF B0 (7:0)
FD OPCOPE DECODE
FD DECODE
IBUF PE
DRAM PE
-INV IBUF
ERROR DECODE
LAT ERROR
10K IBDA
ERROR (C:A)
BUFF ERROR
IFG ERROR SAV LTH IBDA
ERROR SAV
IBUF CONTROL
REVISIONS
CHK CHANGE NO. REV
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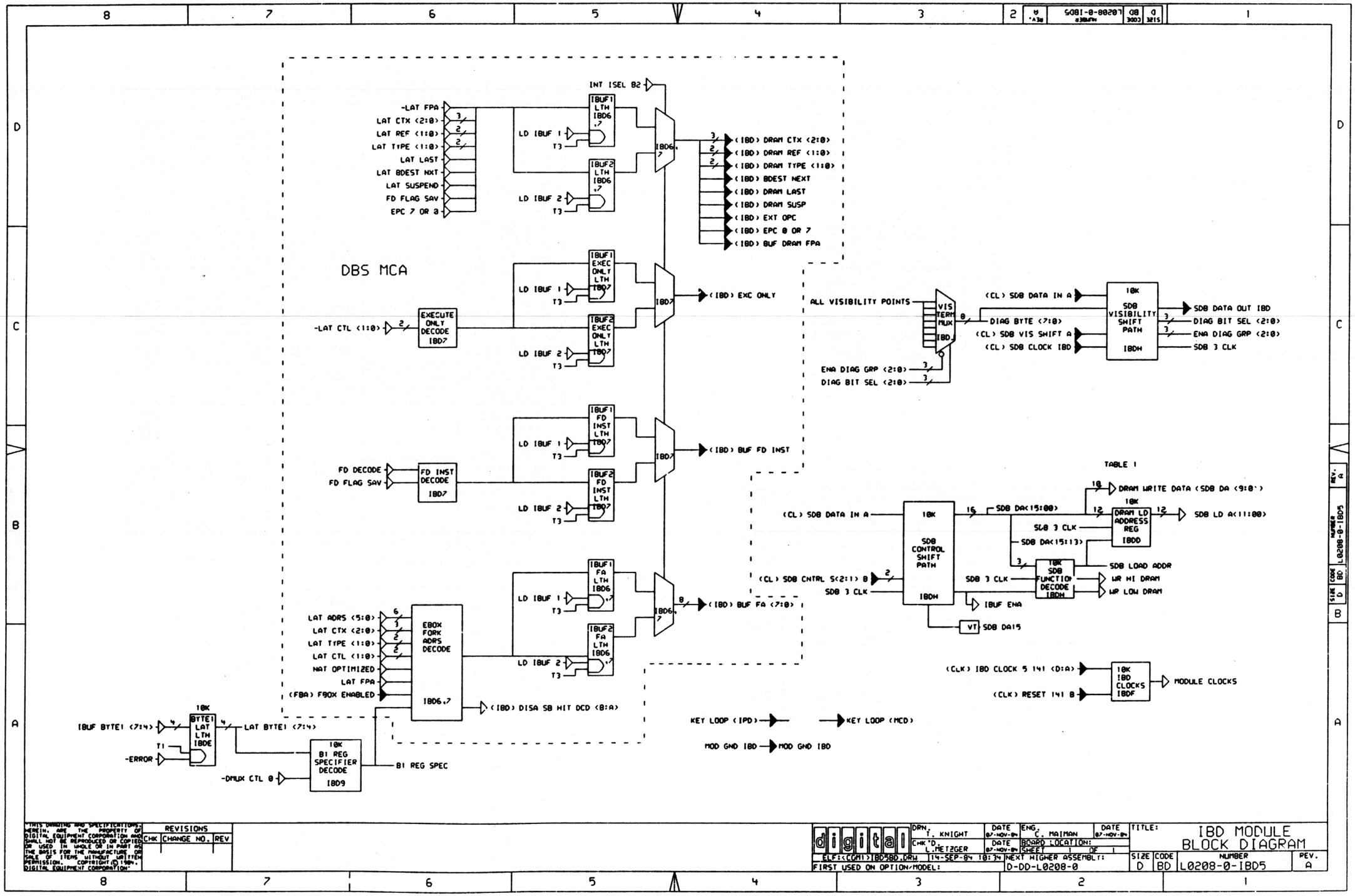
digital
DRN. J.SMITH
DATE 07-NOV-84
CHK'D. L.METZGER
ENG. L. MAIMAN
BOARD LOCATION:
SHEET 1 OF 1
ELF:<COM1>IBD4BD.DRW 14-SEP-84 10:33
NEXT HIGHER ASSEMBLY: D-DD-L0208-6
FIRST USED ON OPTION/MODEL:
TITLE: IBD MODULE BLOCK DIAGRAM
SIZE D
CODE BD
NUMBER L0208-0-IBD4
REV. A

2244



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REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN: T. KNIGHT — DATE: 07-NOV-84
CHK'D: L.METZGER — DATE: 07-NOV-84
ENG: C. MAIMAN — DATE: 07-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF::(COM1)IBD5BD.DRW 14-SEP-84 10:34
NEXT HIGHER ASSEMBLY: D-DD-L0208-0
FIRST USED ON OPTION/MODEL:

TITLE: IBD MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0208-0-IBD5	A

2245

TABLE 1 DRAM BIT FIELDS		
DRAM BIT NAME	DRAM FIELD USE	SDB WRITE GROUP/BIT #
CONTEXT 2 CONTEXT 1 CONTEXT 0	OPERAND SIZE B,W,L,Q,O	HIGH/DA09 HIGH/DA08 HIGH/DA07
TYPE 1 TYPE 0	OPERAND TYPE I,F,G,V	HIGH/DA06 HIGH/DA05
REF 1 REF 0	REF ACCESS R,W,M,A,V	HIGH/DA04 HIGH/DA03
CTL 1 CTL 0	DECODE UNIT CTL E,S,OP2,OP2+EX	HIGH/DA02 HIGH/DA01
SUSP	SUSPEND AFTER	HIGH/DA00
BDEST	BRANCH NEXT	LOW/DA09
LAST	LAST SPECIFIER	LOW/DA08
PAR	ODD PARITY	LOW/DA07
	EBOX FORK ADRS	
FPA FA 5 FA 4 FA 3 FA 2 FA 1 FA 0	ALLOW FPA FORK ADRS 5 FORK ADRS 4 FORK ADRS 3 FORK ADRS 2 FORK ADRS 1 FORK ADRS 0	LOW/DA06 LOW/DA05 LOW/DA04 LOW/DA03 LOW/DA02 LOW/DA01 LOW/DA00

TABLE 2 INSTRUCTION BUFFER (IBUF) FORMATS							
CURRENT SPECIFIER	BYTE 6	BYTE 5	BYTE 4	BYTE 3	BYTE 2	BYTE 1	BYTE 0
SHORT LIT, S# 	- - - -	- - - -	- - - -	- - - -	RMODE RMODE RMODE RMODE	[0,#] [1,#] [2,#] [3,#]	OPCODE OPCODE OPCODE OPCODE
INDEX, I	NOTE 1	-	-	-	BOA	[4,R]	OPCODE
REGISTER, R	-	-	-	-	RMODE	[5,R]	OPCODE
REG DEF, (R)	-	-	-	-	RMODE	[6,R]	OPCODE
AUTO DECR, -(R)	-	-	-	-	RMODE	[7,R]	OPCODE
AUTO INCR, (R)+ R NOT PC IMMED, (PC)+, BYTE IMMED, (PC)+, WORD IMMED, (PC)+, LONG IMMED, (PC)+, QUAD IMMED, (PC)+, OCTA	- - - RMODE NOTE 2 NOTE 3	- - - I†#<B3> I†#<B3> I†#<B3>	- - RMODE I†#<B2> I†#<B2> I†#<B2>	- RMODE I†#<B1> I†#<B1> I†#<B1> I†#<B1>	RMODE I†#<B0> I†#<B0> I†#<B0> I†#<B0> I†#<B0>	[8,R] [8,PC] [8,PC] [8,PC] [8,PC] [8,PC]	OPCODE OPCODE OPCODE OPCODE OPCODE OPCODE
AUTO INCR DEF, @(R)+ R NOT PC ABSOLUTE, @(PC)+	- RMODE	- @#A<B3>	- @#A<B2>	- @#A<B1>	RMODE @#A<B0>	[9,R] [9,PC]	OPCODE OPCODE
BYTE DISP, B†D(R) BYTE DISP DEF, @B†D(R)	- -	- -	- -	RMODE RMODE	B†D<B0> B†D<B0>	[A,R] [B,R]	OPCODE OPCODE
WORD DISP, W†D(R) WORD DISP DEF, @W†D(R)	- -	- -	RMODE RMODE	W†D<B1> W†D<B1>	W†D<B0> W†D<B0>	[C,R] [D,R]	OPCODE OPCODE
LONG DISP, L†D(R) LONG DISP DEF, @L†D(R)	RMODE RMODE	L†D<B3> L†D<B3>	L†D<B2> L†D<B2>	L†D<B1> L†D<B1>	L†D<B0> L†D<B0>	[E,R] [F,R]	OPCODE OPCODE
STRING FORMATS							
1 BYTE STRING 2 BYTE STRING 3 BYTE STRING 4 BYTE STRING	- - - -	- - - -	- - - -	- - - S<B3>	- - S<B2> S<B2>	- S<B1> S<B1> S<B1>	S<B0> S<B0> S<B0> S<B0>
BRANCH FORMATS							
BYTE DISPLACEMENT WORD DISPLACEMENT	- -	- -	- -	- -	- W†D<B1>	B†D<B0> W†D<B0>	OPCODE OPCODE
OPCODE FORMATS							
EXECUTE OPCODE	-	-	-	-	-	-	OPCODE
FD OPCODE	-	-	-	-	-	OPCODE	[F,D]

NOTE 1- BOA CAN BE SEVERAL BYTES IN LENGTH DEPENDING ON SPECIFIER.
NOTE 2- QUAD REQUIRES 2 MEMORY REFERENCES.
NOTE 3- OCTA REQUIRES 4 MEMORY REFERENCES.

[M,R] = [MODE,REG (7:4),(3:0)]

TABLE 3 VENUS BUS FORMATS (FOR IBD)					
BUS FORMAT	SOURCE	BYTE 3	BYTE 2	BYTE 1	BYTE 0
MD BUS, READ MD BUS, WRITE	MCD MOD WR LAT	<B3> <B3>	<B2> <B2>	<B1> <B1>	<B0> <B0>
OP BUS					
MEM FETCH, BYTE MEM FETCH, WORD MEM FETCH, LONG MEM FETCH, QUAD* MEM FETCH, OCTA* STRING, ALL LENGTHS	IMD REG IMD REG IMD REG IMD REG IMD REG IBUF	SEXT SEXT IMD<B3> IMD<B3> IMD<B3> IBUF<B3>	SEXT SEXT IMD<B2> IMD<B2> IMD<B2> IBUF<B2>	SEXT IMD<B1> IMD<B1> IMD<B1> IMD<B1> IBUF<B1>	IMD<B0> IMD<B0> IMD<B0> IMD<B0> IMD<B0> IBUF<B0>
D BUS					
BYTE DISPLACEMENT WORD DISPLACEMENT LONG DISPLACEMENT SHORT LITERAL BYTE IMMEDIATE WORD IMMEDIATE LONG IMMEDIATE QUAD IMMEDIATE* OCTA IMMEDIATE* ABSOLUTE ADRS WRITE DATA	IBUF IBUF IBUF IBUF IBUF IBUF IBUF IBUF IBUF IBUF IDP MOD	SEXT SEXT L†D<B3> ZEXT SEXT SEXT I†#<B3> I†#<B3> I†#<B3> @#A<B3> W<B3>	SEXT SEXT L†D<B2> ZEXT SEXT SEXT I†#<B2> I†#<B2> I†#<B2> @#A<B2> W<B2>	SEXT W†D<B1> L†D<B1> ZEXT SEXT I†#<B1> I†#<B1> I†#<B1> I†#<B1> @#A<B1> W<B1>	B†D<B0> W†D<B0> L†D<B0> S†# I†#<B0> I†#<B0> I†#<B0> I†#<B0> I†#<B0> @#A<B0> W<B0>

*-QUAD REQUIRES 2 MEMORY REFERENCES,
OCTA REQUIRES 4 MEMORY REFERENCES.

TABLE 4 OUTPUT DOUBLE BUFFER USAGE							
SPECIFIERS	IFORK VALID	IFORK BUF 2	IFORK BUF 1	DMUX VA_ID	DMUX BUF 2	DMUX BUF 1	IB STATE
(PC)+, CYCLE 1 QUAD CYCLE 2	1 0	(PC)+ -	- -	1 1	LWD #1 -	- LWD #2	1 0
B†D(R)	1	B†(R)	-	1	†B DISP	-	0
(PC)+, CYCLE 1	1	(PC)+	-	1	LWD #1	-	1
OCTA CYCLE 2	0	-	-	1	-	LWD #2	1
CYCLE 3	0	-	-	1	LWD #3	-	1
CYCLE 4	0	-	-	1	-	LWD #4	0
REGISTER MODE	1	R	-	0	-	-	0
DRAIN, WITHOUT LD IFORK DISP, OR NOT ENOUGH BYTES	0	-	-	0	-	-	0
S#, SHORT LITERAL	1	S#	-	1	LITERAL	-	0

NOTE - THIS TABLE SHOWS EXAMPLES OF DOUBLE BUFFER USAGE.

REVISIONS

CHK	CHANGE NO.	REV

digital

DRN. J.SMITH DATE 07-NOV-84
CHK'D L.METZGER DATE 07-NOV-84
ENG. C. MAIMAN DATE 07-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:(COM)IBD68D.DRW 14-SEP-84 10:35
NEXT HIGHER ASSEMBLY: D-DD-L0208-0
FIRST USED ON OPTION/MODEL:

TITLE: IBD MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0208-0-IBD6	H

2246

TABLE 5
BUS PARITY BIT FORMATS

BUS FORMAT	SOURCE	PARITY BYTE 3	PARITY BYTE 2	PARITY BYTE 1	PARITY BYTE 0	LONGWD PARITY
MD BUS, READ	MCD MOD	<B3>	<B2>	<B1>	<B0>	N/A
MD BUS, WRITE PARITY DIRECT TO MBOX FROM EBOX	-	NOT ON IBD	NOT ON IBD	NOT ON IBD	NOT ON IBD	N/A
OP BUS, LWD OPAR ONLY						
MEM FETCH, BYTE	IMD REG	1	1	1	IMD<B0>	LWD OPAR
MEM FETCH, WORD	IMD REG	1	1	IMD<B1>	IMD<B0>	LWD OPAR
MEM FETCH, LONG	IMD REG	IMD<B3>	IMD<B2>	IMD<B1>	IMD<B0>	LWD OPAR
MEM FETCH, QUAD*	IMD REG	IMD<B3>	IMD<B2>	IMD<B1>	IMD<B0>	LWD OPAR
MEM FETCH, OCTA*	IMD REG	IMD<B3>	IMD<B2>	IMD<B1>	IMD<B0>	LWD OPAR
STRING, 1 BYTE	IBUF	N/A	N/A	N/A	IBUF<B0>	LWD OPAR
STRING, 2 BYTE	IBUF	N/A	N/A	IBUF<B1>	IBUF<B0>	LWD OPAR
STRING, 3 BYTE	IBUF	N/A	IBUF<B2>	IBUF<B1>	IBUF<B0>	LWD OPAR
STRING, 4 BYTE	IBUF	IBUF<B3>	IBUF<B2>	IBUF<B1>	IBUF<B0>	LWD OPAR
D BUS						
BYTE BRANCH DISP.	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B2>	IBUF<B1>	N/A
WORD BRANCH DISP.	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B2>	IBUF<B1>	N/A
BYTE DISPLACEMENT	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
WORD DISPLACEMENT	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
LONG DISPLACEMENT	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
SHORT LITERAL	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B2>	IBUF<B1>	N/A
BYTE IMMEDIATE	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
WORD IMMEDIATE	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
LONG IMMEDIATE	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
QUAD IMMEDIATE*	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
OCTA IMMEDIATE*	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A
ABSOLUTE ADRS	IBUF	IBUF<B5>	IBUF<B4>	IBUF<B3>	IBUF<B2>	N/A

* - QUAD REQUIRES 2 MEMORY REFERENCES,
OCTA REQUIRES 4 MEMORY REFERENCES.

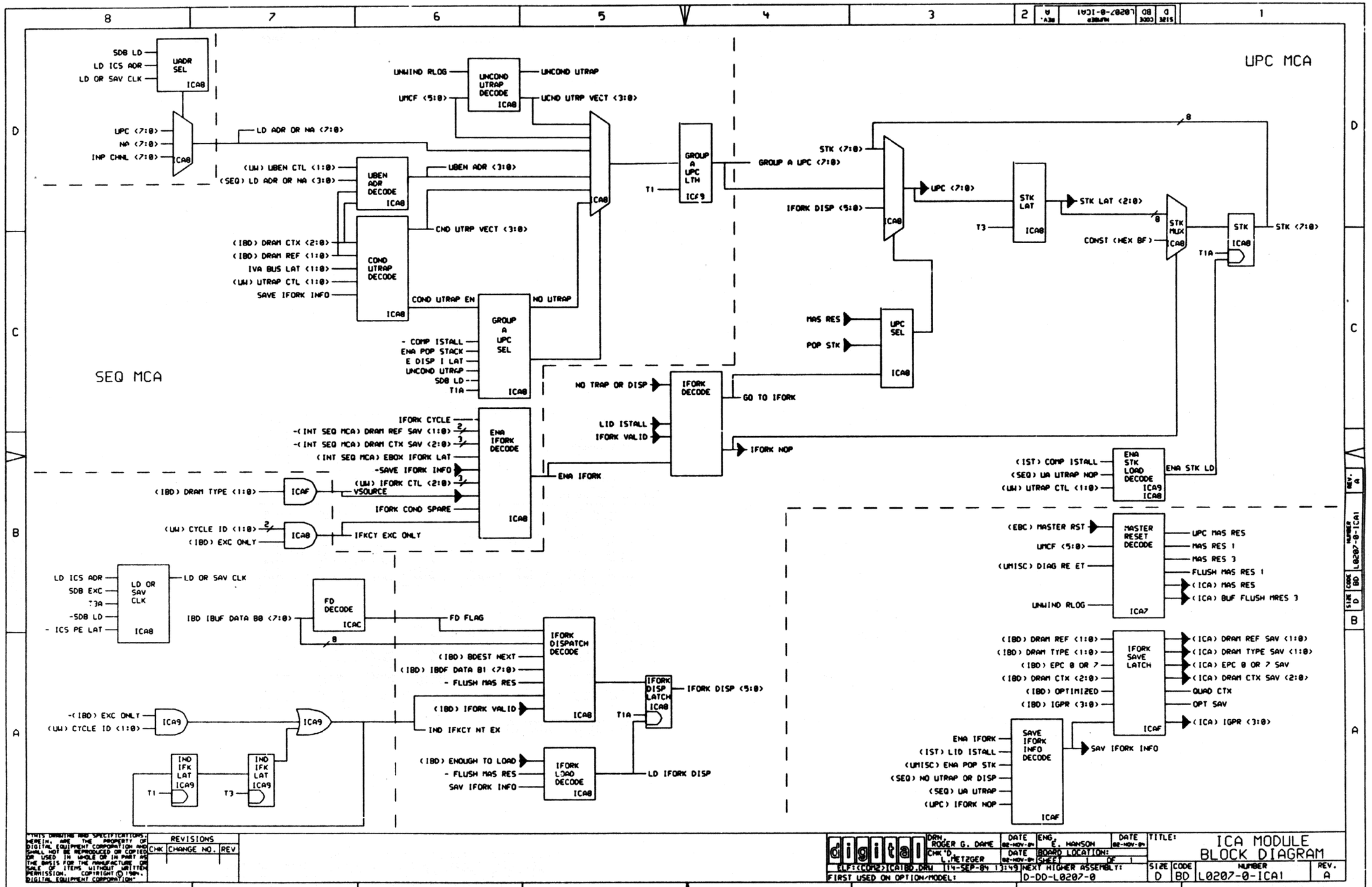
REVISIONS
CHK | CHANGE NO. | REV

digital
DRN. J.SMITH DATE 07-NOV-84
CHK'D L.METZGER DATE 07-NOV-84
ELF:(COM1)IBD780.DRW 14-SEP-84 10:16
FIRST USED ON OPTION/MODEL:
ENG. C. MAIMAN DATE 07-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
NEXT HIGHER ASSEMBLY: D-DD-L0208-0

TITLE: IBD MODULE BLOCK DIAGRAM
SIZE D | CODE BD | NUMBER L0208-0-IBD7 | REV. A

SIZE D | CODE BD | NUMBER L0208-0-IBD7 | REV. A

2247


UPC MCA
SEQ MCA
UADR SEL
ICA8
UPC (7:0)
NA (7:0)
INP CHNL (7:0)
LD ADR OR NA (7:0)
UNCOND UTRAP DECODE
UNWIND RLOG
UMCF (5:0)
UNCOND UTRAP
UCND UTRP VECT (3:0)
UBEN ADR DECODE
(UW) UBEN CTL (1:0)
(SEQ) LD ADR OR NA (3:0)
UBEN ADR (3:0)
COND UTRAP DECODE
(IBD) DRAM CTX (2:0)
(IBD) DRAM REF (1:0)
IVA BUS LAT (1:0)
(UW) UTRAP CTL (1:0)
SAVE IFORK INFO
CND UTRP VECT (3:0)
COND UTRAP EN
NO UTRAP
GROUP A UPC SEL
- COMP ISTALL
ENA POP STACK
E DISP I LAT
UNCOND UTRAP
SDB LD
T1A
GROUP A UPC LTH
ICF9
T1
GROUP A UPC (7:0)
STK (7:0)
IFORK DISP (5:0)
UPC (7:0)
STK LAT
T3
STK LAT (2:0)
STK MUX
CONST (HEX BF)
STK
STK (7:0)
MAS RES
POP STK
UPC SEL
NO TRAP OR DISP
IFORK DECODE
GO TO IFORK
LID ISTALL
IFORK VALID
IFORK NOP
IFORK CYCLE
-(INT SEQ MCA) DRAM REF SAV (1:0)
-(INT SEQ MCA) DRAM CTX SAV (2:0)
(INT SEQ MCA) EBOX IFORK LAT
-SAVE IFORK INFO
(UW) IFORK CTL (2:0)
VSOURCE
IFORK COND SPARE
ENA IFORK DECODE
ENA IFORK
(IBD) DRAM TYPE (1:0)
ICAF
(UW) CYCLE ID (1:0)
(IBD) EXC ONLY
IFKCY EXC ONLY
(IST) COMP ISTALL
(SEQ) UA UTRAP NOP
(UW) UTRAP CTL (1:0)
ENA STK LOAD DECODE
ICA9
ENA STK LD
LD ICS ADR
SDB EXC
T3A
-SDB LD
- ICS PE LAT
LD OR SAV CLK
LD OR SAV CLK
IBD IBUF DATA B0 (7:0)
FD DECODE
ICAC
FD FLAG
IFORK DISPATCH DECODE
(IBD) BDEST NEXT
(IBD) IBDF DATA B1 (7:0)
- FLUSH MAS RES
(IBD) IFORK VALID
IND IFKCY NT EX
IFORK DISP LATCH
IFORK DISP (5:0)
T1A
-(IBD) EXC ONLY
(UW) CYCLE ID (1:0)
IND IFK LAT
T1
T3
(IBD) ENOUGH TO LOAD
- FLUSH MAS RES
SAV IFORK INFO
IFORK LOAD DECODE
LD IFORK DISP
(EBC) MASTER RST
UMCF (5:0)
(UMISC) DIAG RE ET
UNWIND RLOG
MASTER RESET DECODE
ICA7
UPC MAS RES
MAS RES 1
MAS RES 3
FLUSH MAS RES 1
(ICA) MAS RES
(ICA) BUF FLUSH MRES 3
(IBD) DRAM REF (1:0)
(IBD) DRAM TYPE (1:0)
(IBD) EPC 0 OR 7
(IBD) DRAM CTX (2:0)
(IBD) OPTIMIZED
(IBD) IGPR (3:0)
IFORK SAVE LATCH
(ICA) DRAM REF SAV (1:0)
(ICA) DRAM TYPE SAV (1:0)
(ICA) EPC 0 OR 7 SAV
(ICA) DRAM CTX SAV (2:0)
QUAD CTX
OPT SAV
(ICA) IGPR (3:0)
ENA IFORK
(IST) LID ISTALL
(UMISC) ENA POP STK
(SEQ) NO UTRAP OR DISP
(SEQ) UA UTRAP
(UPC) IFORK NOP
SAVE IFORK INFO DECODE
SAV IFORK INFO
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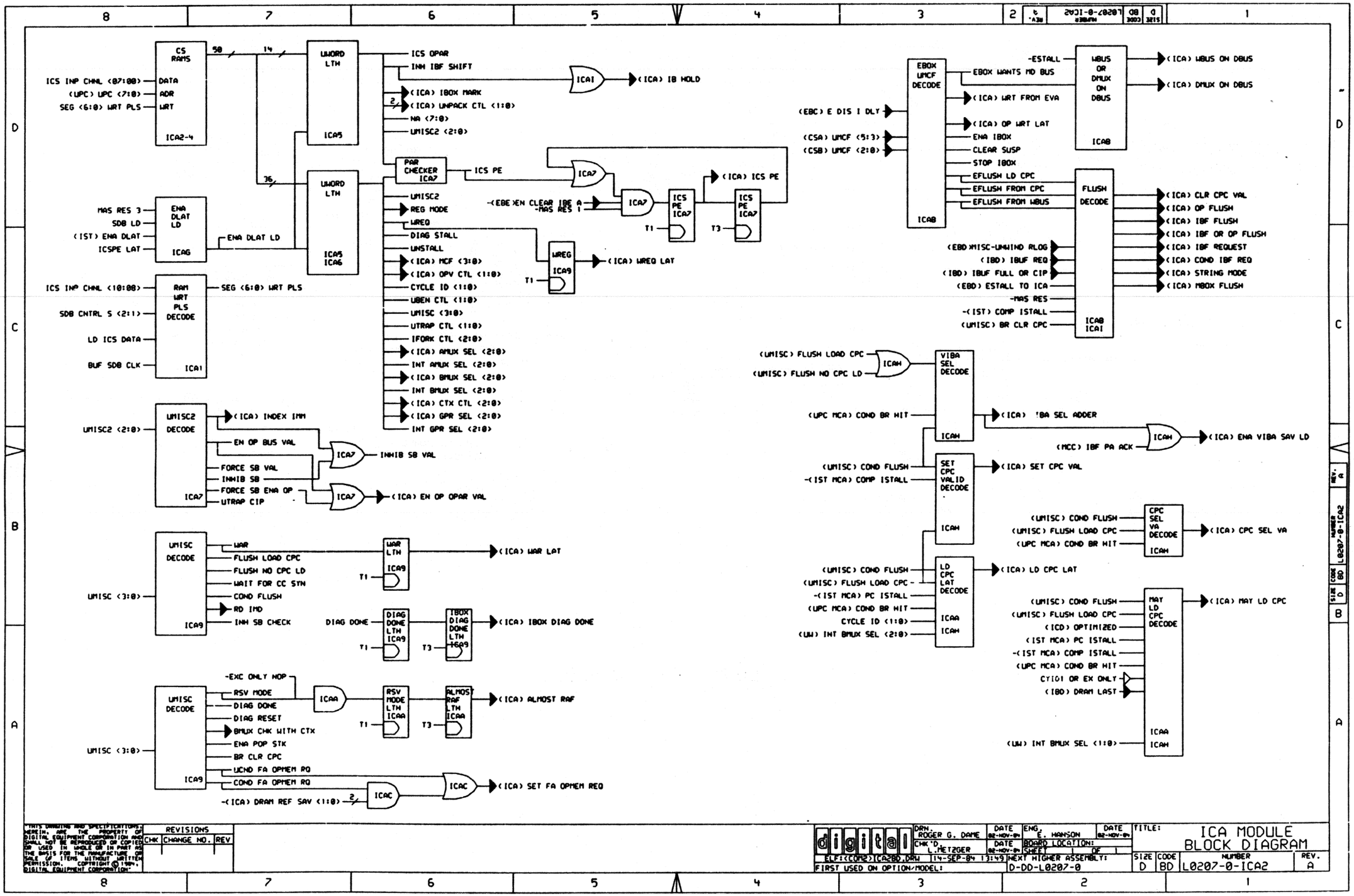
REVISIONS
CHK
CHANGE NO.
REV
digital
DRN. ROGER G. DAME
CHK'D L.METZGER
DATE 02-NOV-84
ENG. E. HANSON
DATE 02-NOV-84
DATE 02-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:(COM2)ICABD.DRW 14-SEP-84 13:49
NEXT HIGHER ASSEMBLY: D-DD-L0207-0
FIRST USED ON OPTION/MODEL:
TITLE: ICA MODULE BLOCK DIAGRAM
SIZE D
CODE BD
NUMBER L0207-0-ICA1
REV. A

[redacted]



REVISIONS		
CHK	CHANGE NO.	REV

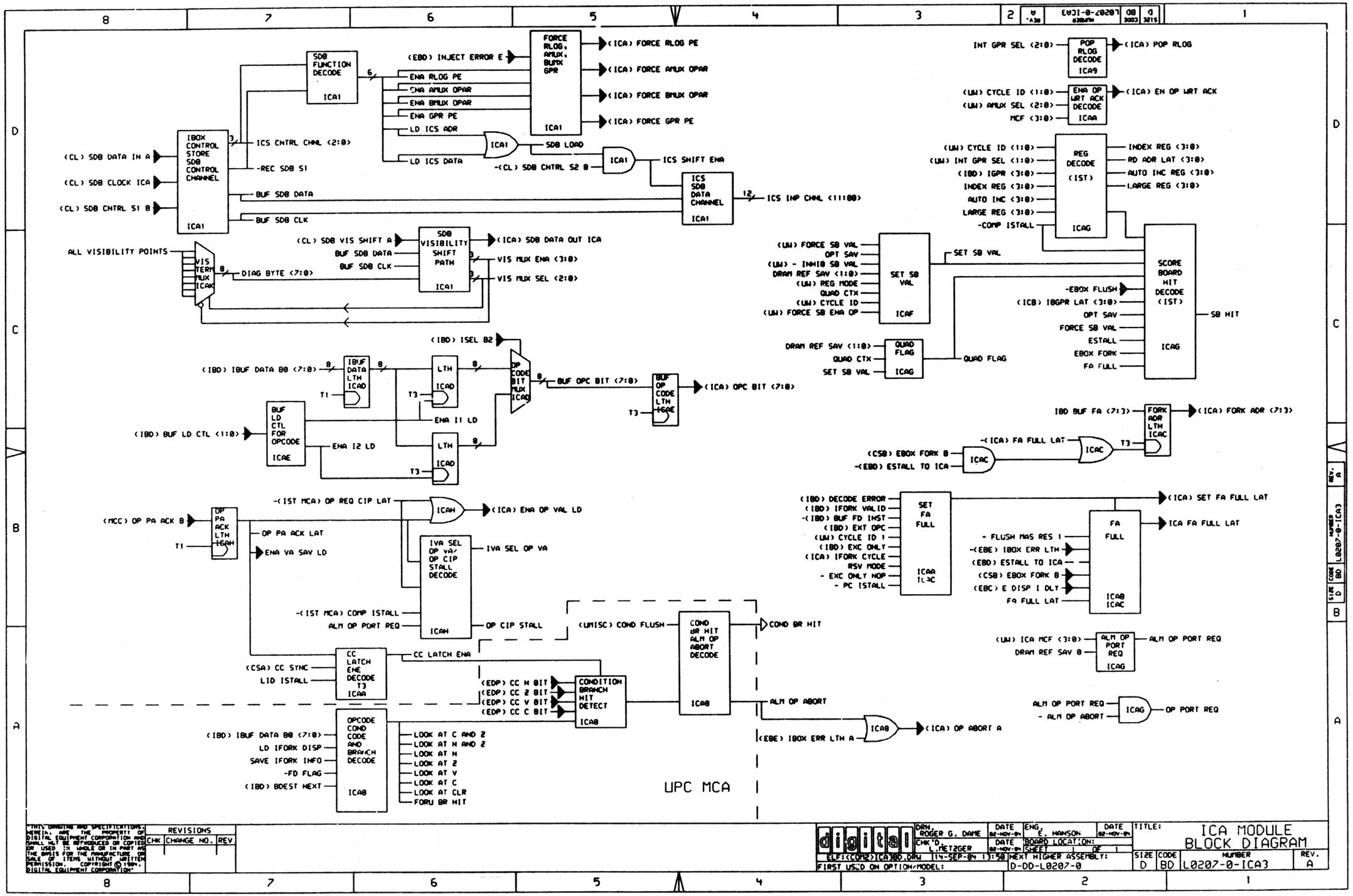
digital

DRN. ROGER G. DAME — DATE 02-NOV-84 — ENG. E. HANSON — DATE 02-NOV-84
CHK'D L. METZGER — DATE 02-NOV-84 — BOARD LOCATION:
ELPI(COM2)ICA2BD.DRW 14-SEP-84 13:49 — SHEET 1 OF
FIRST USED ON OPTION/MODEL: — NEXT HIGHER ASSEMBLY: D-DD-L0207-0

TITLE: ICA MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0207-0-ICA2	A

2249


SDB FUNCTION DECODE ICA1
(EBD) INJECT ERROR E
ENA RLOG PE
ENA AMUX OPAR
ENA BMUX OPAR
ENA GPR PE
LD ICS ADR
LD ICS DATA
FORCE RLOG, AMUX, BUFX GPR ICA1
(ICA) FORCE RLOG PE
(ICA) FORCE AMUX OPAR
(ICA) FORCE BMUX OPAR
(ICA) FORCE GPR PE
SDB LOAD
-(CL) SDB CNTRL S2 B
ICS SHIFT ENA
IBOX CONTROL STORE SDB CONTROL CHANNEL ICA1
(CL) SDB DATA IN A
(CL) SDB CLOCK ICA
(CL) SDB CNTRL S1 B
ICS CNTRL CHNL (2:0)
-REC SDB S1
BUF SDB DATA
BUF SDB CLK
ICS SDB DATA CHANNEL ICA1
ICS INP CHNL (11:00)
ALL VISIBILITY POINTS
VIS TERM MUX ICAK
DIAG BYTE (7:0)
(CL) SDB VIS SHIFT A
SDB VISIBILITY SHIFT PATH ICA1
(ICA) SDB DATA OUT ICA
VIS MUX ENA (3:0)
VIS MUX SEL (2:0)
(IBD) ISEL B2
(IBD) IBUF DATA B0 (7:0)
IBUF DATA LTH ICAD
LTH ICAD
OP CODE BIT MUX ICAG
BUF OPC BIT (7:0)
BUF OP CODE LTH 1GAE
(ICA) OPC BIT (7:0)
(IBD) BUF LD CTL (1:0)
BUF LD CTL FOR OPCODE ICAE
ENA I1 LD
ENA I2 LD
-(IST MCA) OP REQ CIP LAT
ICAH
(ICA) ENA OP VAL LD
(MCC) OP PA ACK B
OP PA ACK LTH ICAH
OP PA ACK LAT
ENA VA SAV LD
IVA SEL OP VA/ OP CIP STALL DECODE ICAH
IVA SEL OP VA
-(IST MCA) COMP ISTALL
ALM OP PORT REQ
OP CIP STALL
(UMISC) COND FLUSH
COND BR HIT ALM OP ABORT DECODE ICA8
COND BR HIT
ALM OP ABORT
(CSA) CC SYNC
LID ISTALL
CC LATCH ENE DECODE T3 ICAA
CC LATCH ENA
(EDP) CC N BIT
(EDP) CC Z BIT
(EDP) CC V BIT
(EDP) CC C BIT
CONDITION BRANCH HIT DETECT ICA8
(IBD) IBUF DATA B0 (7:0)
LD IFORK DISP
SAVE IFORK INFO
-FD FLAG
(IBD) BDEST NEXT
OPCODE COND CODE AND BRANCH DECODE ICA8
LOOK AT C AND Z
LOOK AT N AND Z
LOOK AT N
LOOK AT Z
LOOK AT V
LOOK AT C
LOOK AT CLR
FORU BR HIT
UPC MCA
INT GPR SEL (2:0)
POP RLOG DECODE ICA9
(ICA) POP RLOG
(UM) CYCLE ID (1:0)
(UM) AMUX SEL (2:0)
MCF (3:0)
ENA OP WRT ACK DECODE ICAA
(ICA) EN OP WRT ACK
(UM) INT GPR SEL (1:0)
(IBD) IGPR (3:0)
INDEX REG (3:0)
AUTO INC (3:0)
LARGE REG (3:0)
-COMP ISTALL
REG DECODE (IST) ICAG
INDEX REG (3:0)
RD ADR LAT (3:0)
AUTO INC REG (3:0)
LARGE REG (3:0)
(UM) FORCE SB VAL
OPT SAV
(UM) - INHIB SB VAL
DRAM REF SAV (1:0)
(UM) REG MODE
QUAD CTX
(UM) CYCLE ID
(UM) FORCE SB ENA OP
SET SB VAL ICAF
SET SB VAL
DRAM REF SAV (1:0)
QUAD CTX
SET SB VAL
QUAD FLAG ICAG
QUAD FLAG
-EBOX FLUSH
(ICB) IBGPR LAT (3:0)
OPT SAV
FORCE SB VAL
ESTALL
EBOX FORK
FA FULL
SCORE BOARD HIT DECODE (IST) ICAG
SB HIT
IBD BUF FA (7:3)
FORK ADR LTH ICAC
(ICA) FORK ADR (7:3)
-(ICA) FA FULL LAT
(CSB) EBOX FORK B
-(EBD) ESTALL TO ICA
ICAC
T3
(IBD) DECODE ERROR
(IBD) IFORK VALID
-(IBD) BUF FD INST
(IBD) EXT OPC
(UM) CYCLE ID 1
(IBD) EXC ONLY
(ICA) IFORK CYCLE
RSV MODE
- EXC ONLY NOP
- PC ISTALL
SET FA FULL ICAA ICAC
(ICA) SET FA FULL LAT
ICA FA FULL LAT
- FLUSH MAS RES 1
-(EBE) IBOX ERR LTH
(EBD) ESTALL TO ICA
(CSB) EBOX FORK B
(EBC) E DISP 1 DLY
FA FULL LAT
FA FULL ICA8 ICAC
(UM) ICA MCF (3:0)
DRAM REF SAV 0
ALM OP PORT REQ ICAG
ALM OP PORT REQ
ALM OP PORT REQ
- ALM OP ABORT
ICAG
OP PORT REQ
(EBE) IBOX ERR LTH A
ICA8
(ICA) OP ABORT A
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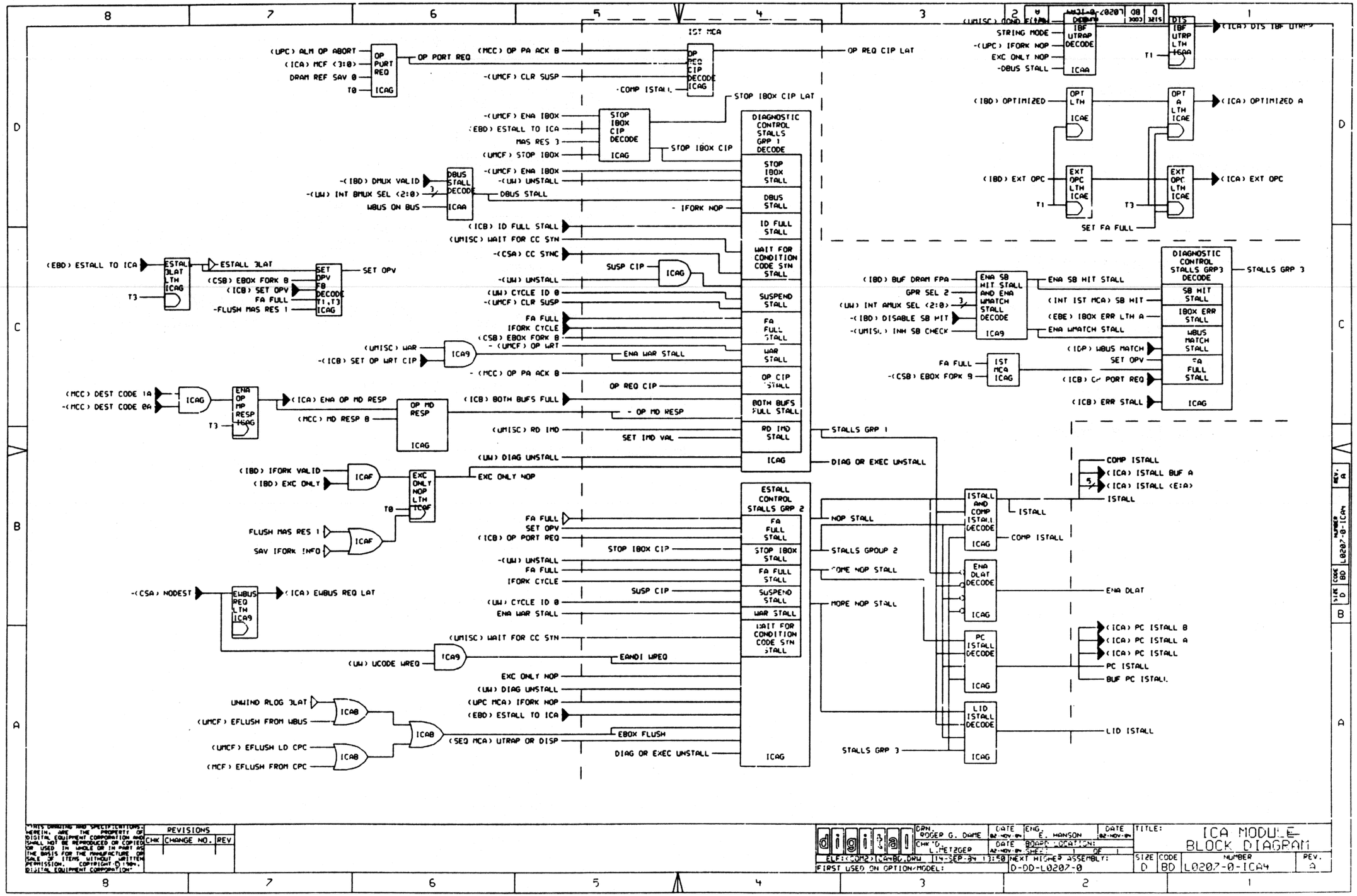
REVISIONS
CHK CHANGE NO. REV
digital
DRN. ROGER G. DAME
DATE 02-NOV-84
ENG. E. HANSON
DATE 02-NOV-84
CHK'D. L.METZGER
DATE 02-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:(COM2)ICA3BD.DRW 14-SEP-84 13:58
NEXT HIGHER ASSEMBLY: D-DD-L0207-0
FIRST USED ON OPTION/MODEL:
TITLE: ICA MODULE BLOCK DIAGRAM
SIZE D
CODE BD
NUMBER L0207-0-ICA3
REV. A



REVISIONS

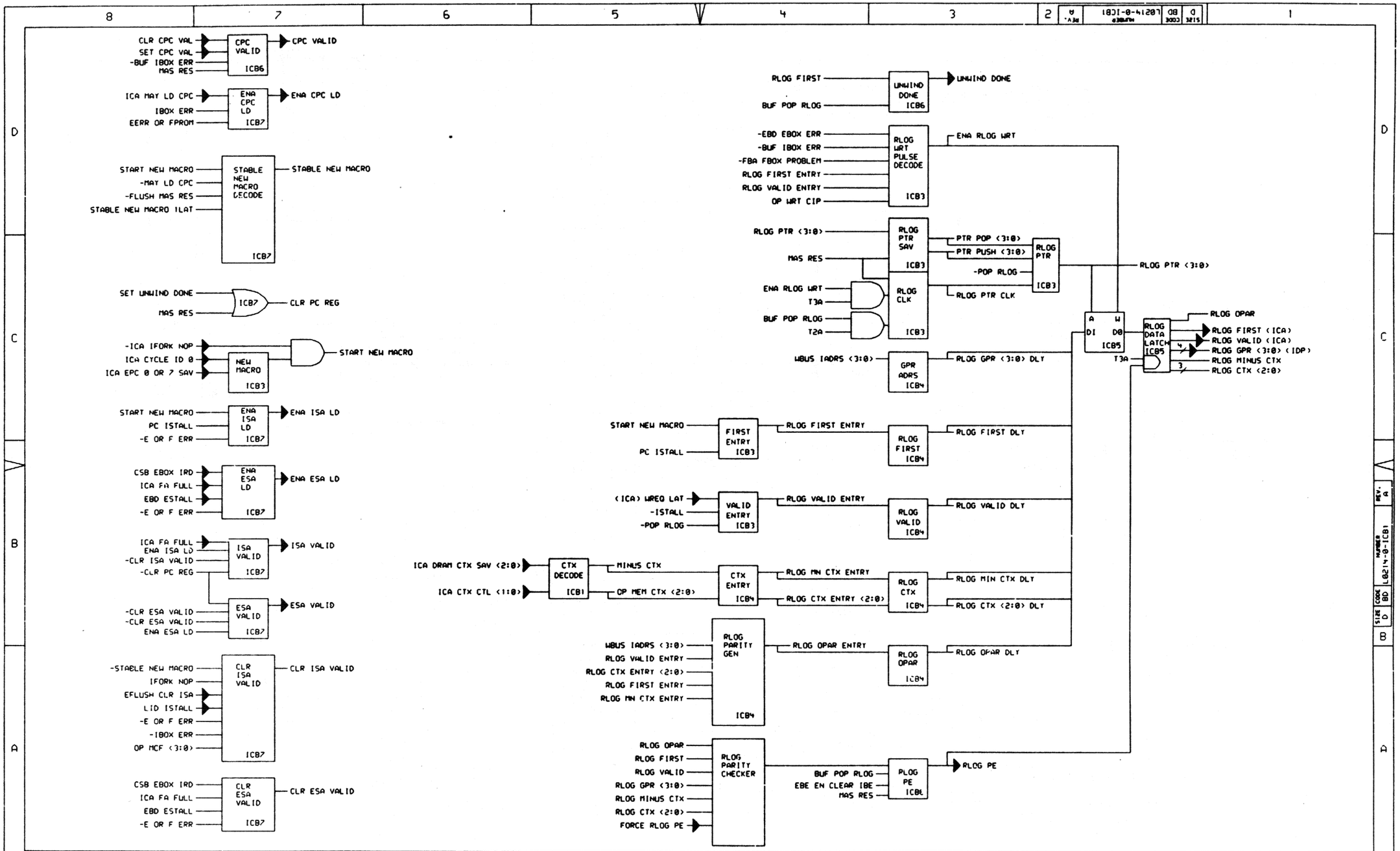
CHK	CHANGE NO.	REV

DRN ROGER G. DUME	DATE 02-NOV-84	ENG E. HANSON	DATE 02-NOV-84
CHK TO L. METZGER	DATE 02-NOV-84	BOARD LOCATION:	
ELP:(COM2)LCAMBD.DRW 14-SEP-84 13:50		SHT: 1 OF 1	
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-L0207-0	

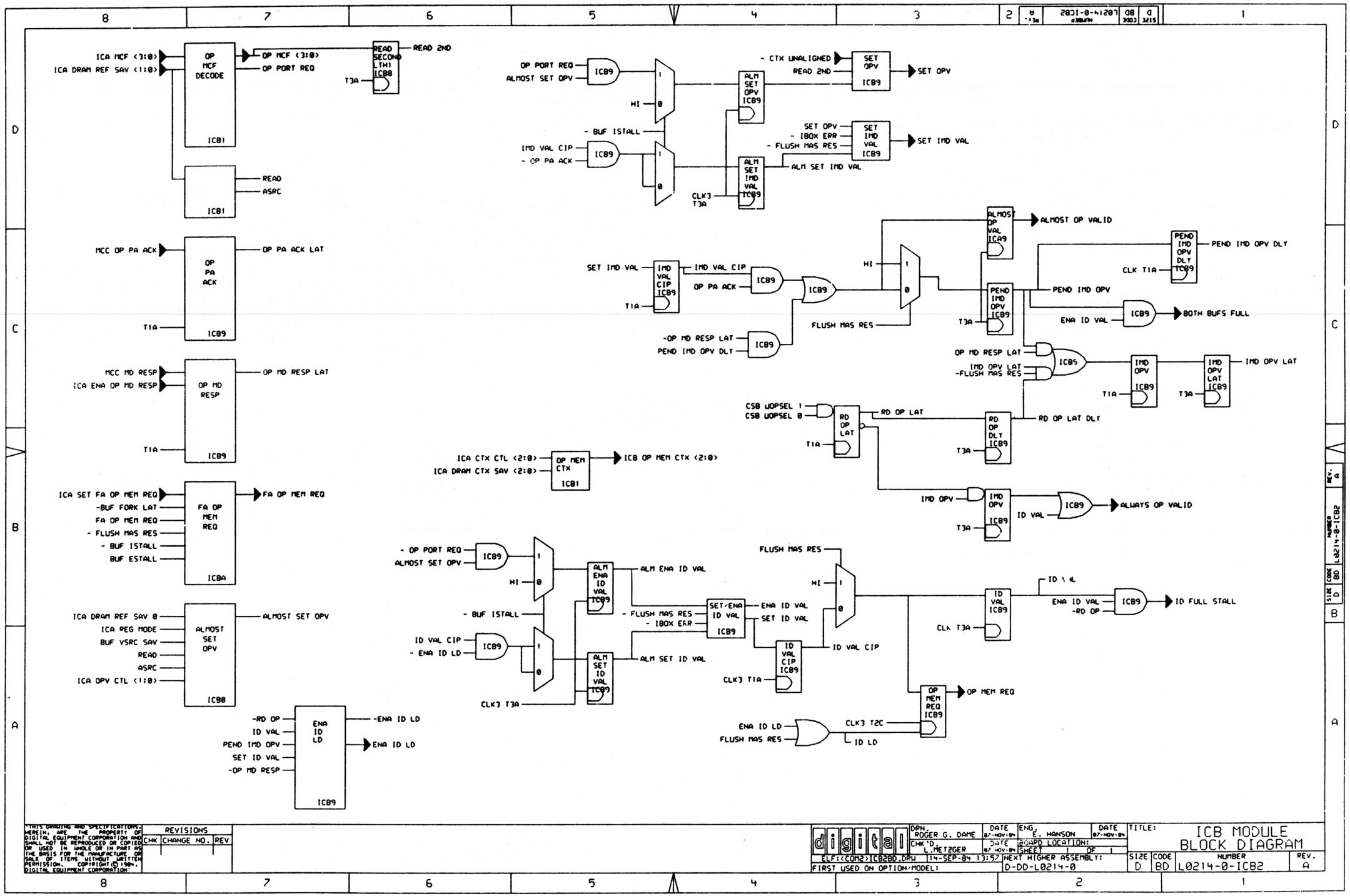
TITLE: ICA MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0207-0-ICA4	A

2251



2252



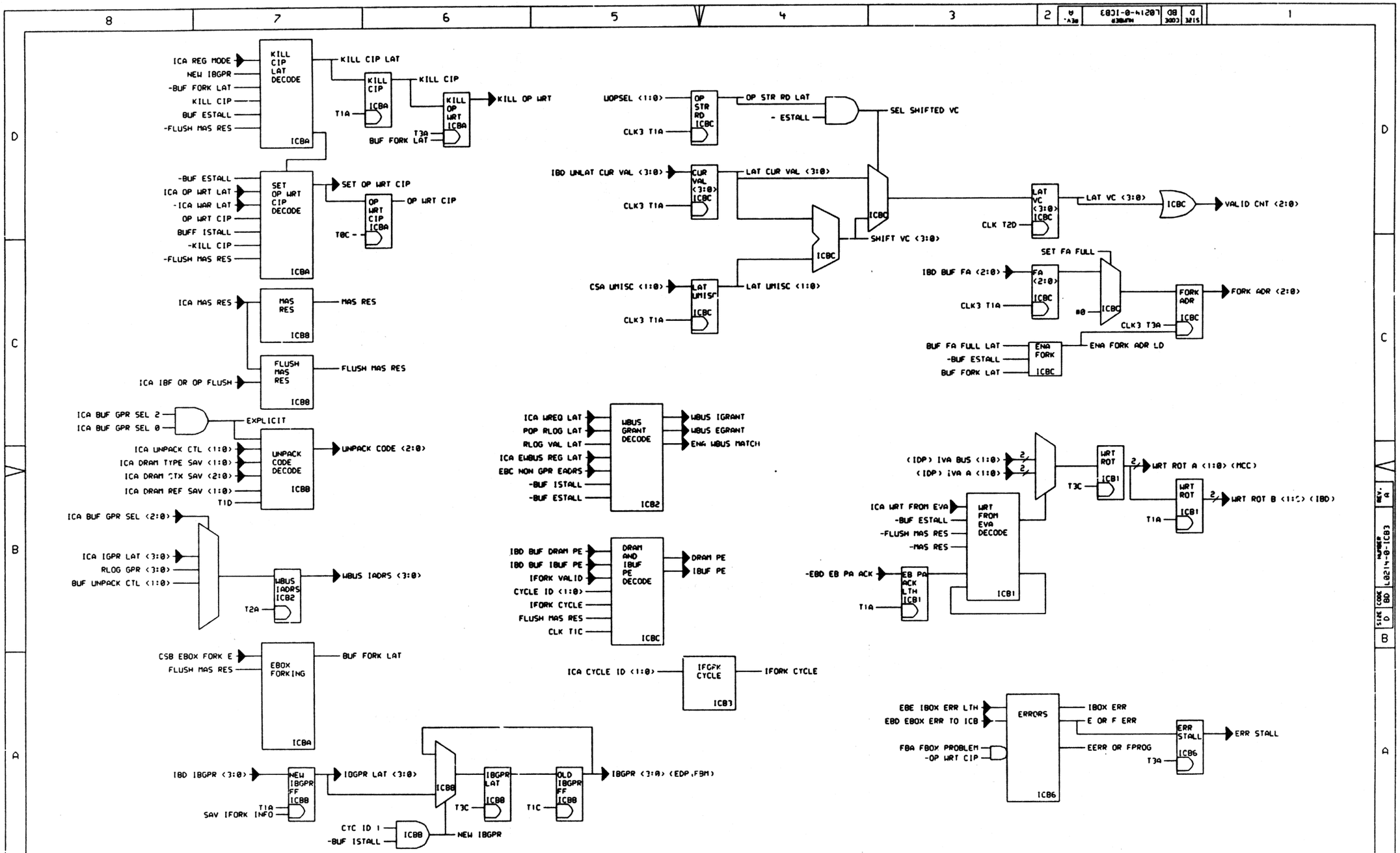
REVISIONS		
CHK	CHANGE NO.	REV

DRN. ROGER G. DAME	DATE 07-NOV-84	ENG. E. HANSON	DATE 07-NOV-84
CHK'D. L.METZGER	DATE 07-NOV-84	PWB PD LOCATION:	
ELF:<COM2>ICB2BD.DPW 14-SEP-84 13:57		SHEET 1 OF 1	
FIRST USED ON OPTION/MODEL:		NEXT HIGHER ASSEMBLY: D-DD-L0214-0	

TITLE: ICB MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0214-0-ICB2	A

2253


ICA REG MODE
NEW IBGPR
-BUF FORK LAT
KILL CIP
BUF ESTALL
-FLUSH MAS RES
KILL CIP LAT DECODE
ICBA
KILL CIP LAT
KILL CIP
T1A
KILL OP WRT ICBA
KILL OP WRT
BUF FORK LAT
T3A
-BUF ESTALL
ICA OP WRT LAT
-ICA WAR LAT
OP WRT CIP
BUFF ISTALL
-KILL CIP
-FLUSH MAS RES
SET OP WRT CIP DECODE
SET OP WRT CIP
OP WRT CIP ICBA
T8C -
ICA MAS RES
MAS RES ICB8
MAS RES
FLUSH MAS RES ICB8
ICA IBF OR OP FLUSH
FLUSH MAS RES
ICA BUF GPR SEL 2
ICA BUF GPR SEL 0
EXPLICIT
ICA UNPACK CTL (1:0)
ICA DRAM TYPE SAV (1:0)
ICA DRAM CTX SAV (2:0)
ICA DRAM REF SAV (1:0)
T1D
UNPACK CODE DECODE ICB8
UNPACK CODE (2:0)
ICA BUF GPR SEL (2:0)
ICA IGPR LAT (3:0)
RLOG GPR (3:0)
BUF UNPACK CTL (1:0)
WBUS IADRS ICB2
T2A
WBUS IADRS (3:0)
CSB EBOX FORK E
FLUSH MAS RES
EBOX FORKING ICBA
BUF FORK LAT
IBD IBGPR (3:0)
NEW IBGPR FF ICB8
IBGPR LAT (3:0)
SAV IFORK INFO
T1A
ICB8
T3C
IBGPR LAT ICB8
T1C
OLD IBGPR FF ICB8
IBGPR (3:A) (EDP,FBM)
CYC ID 1
-BUF ISTALL
NEW IBGPR
UOPSEL (1:0)
CLK3 T1A
OP STR RD ICBC
OP STR RD LAT
- ESTALL
SEL SHIFTED VC
IBD UNLAT CUR VAL (3:0)
CUR VAL (3:0) ICBC
LAT CUR VAL (3:0)
ICBC
SHIFT VC (3:0)
CSA UMISC (1:0)
LAT UMISC ICBC
LAT UMISC (1:0)
LAT VC (3:0) ICBC
CLK T2D
LAT VC (3:0)
ICBC
VALID CNT (2:0)
SET FA FULL
IBD BUF FA (2:0)
FA (2:0) ICBC
#0
ICBC
FORK ADR ICBC
FORK ADR (2:0)
CLK3 T3A
BUF FA FULL LAT
-BUF ESTALL
BUF FORK LAT
ENA FORK ICBC
ENA FORK ADR LD
ICA WREQ LAT
POP RLOG LAT
RLOG VAL LAT
ICA EWBUS REG LAT
EBC NON GPR EADRS
-BUF ISTALL
-BUF ESTALL
WBUS GRANT DECODE ICB2
WBUS IGRANT
WBUS EGRANT
ENG WBUS MATCH
IBD BUF DRAM PE
IBD BUF IBUF PE
IFORK VALID
CYCLE ID (1:0)
IFORK CYCLE
FLUSH MAS RES
CLK T1C
DRAM AND IBUF PE DECODE ICBC
DRAM PE
IBUF PE
ICA CYCLE ID (1:0)
IFORK CYCLE ICB7
IFORK CYCLE
(IDP) IVA BUS (1:0)
(IDP) IVA A (1:0)
WRT ROT ICB1
T3C
WRT ROT A (1:0) (MCC)
WRT ROT ICB1
T1A
WRT ROT B (1:0) (IBD)
ICA WRT FROM EVA
-BUF ESTALL
-FLUSH MAS RES
-MAS RES
WRT FROM EVA DECODE ICB1
-EBD EB PA ACK
EB PA ACK LTH ICB1
T1A
EBE IBOX ERR LTH
EBD EBOX ERR TO ICB
FBA FBOX PROBLEM
-OP WRT CIP
ERRORS ICB6
IBOX ERR
E OR F ERR
EERR OR FPROG
ERR STALL ICB6
T3A
ERR STALL
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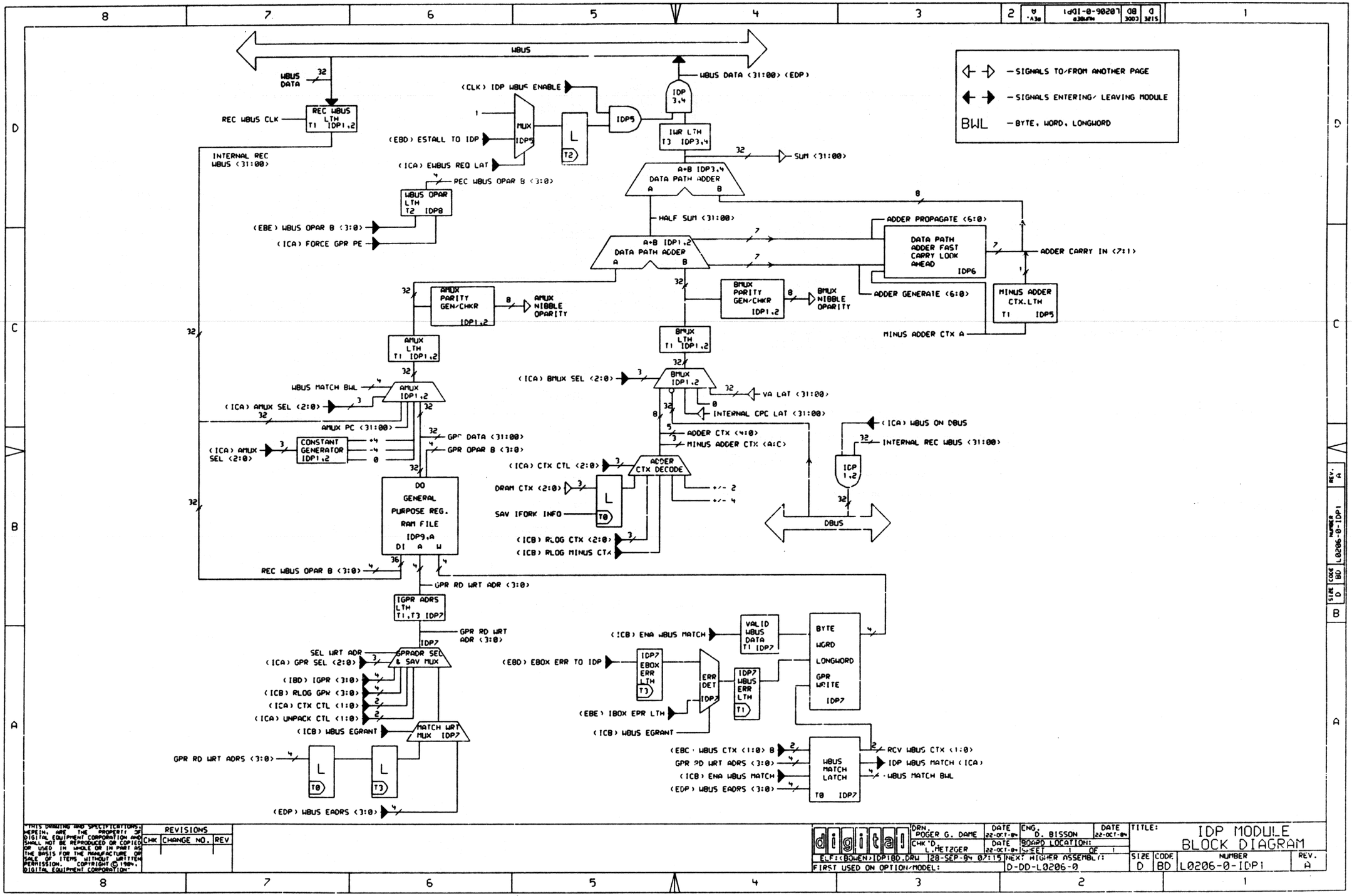
REVISIONS
CHK CHANGE NO. REV
digital
DRN. ROGER S. DAME
DATE 07-NOV-84
ENG. E. HANSON
DATE 07-NOV-84
CHK D. L.METZGER
DATE 07-NOV-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:[COM2]ICB3BD.DPW 14-SEP-84 13:52
NEXT HIGHER ASSEMBLY:
FIRST USED ON OPTION/MODEL:
D-DD-L0214-0
TITLE: ICB MODULE BLOCK DIAGRAM
SIZE D
CODE BD
NUMBER L0214-0-ICB3
REV. A



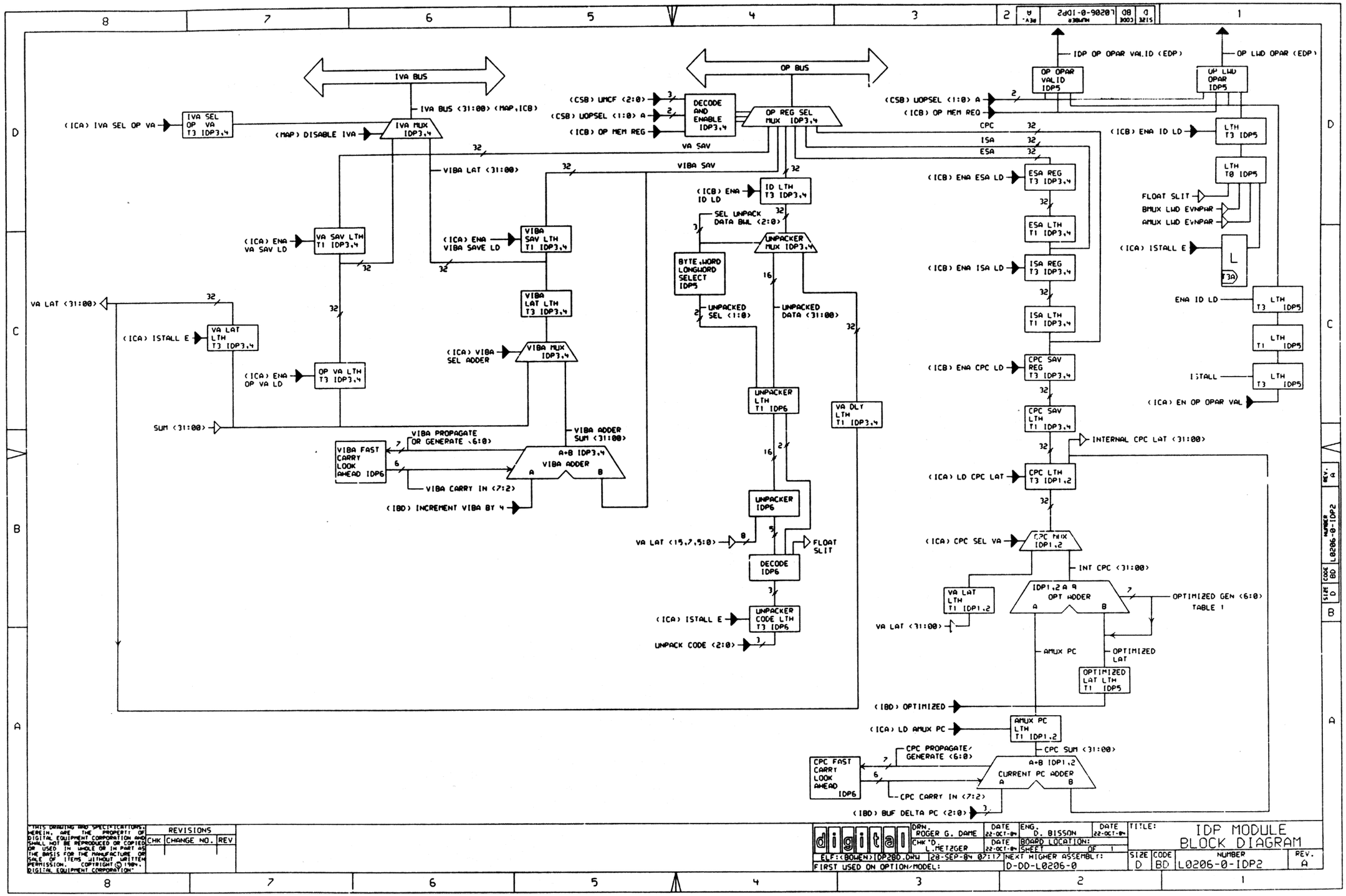
REVISIONS		
CHK	CHANGE NO.	REV

DRN. ROGER G. DAME	DATE 22-OCT-84	ENG. D. BISSON	DATE 22-OCT-84
CHK D. L.METZGER	DATE 22-OCT-84	BOARD LOCATION:	
		SHEET 1 OF 1	
E.L.F:<BOWEN>IDP1BD.DRW 28-SEP-84 07:15		NEXT HIGHER ASSEMBLY:	
FIRST USED ON OPTION/MODEL:		D-DD-L0206-0	

TITLE: IDP MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0206-0-IDP1	A

2255



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REVISIONS		
CHK	CHANGE NO.	REV

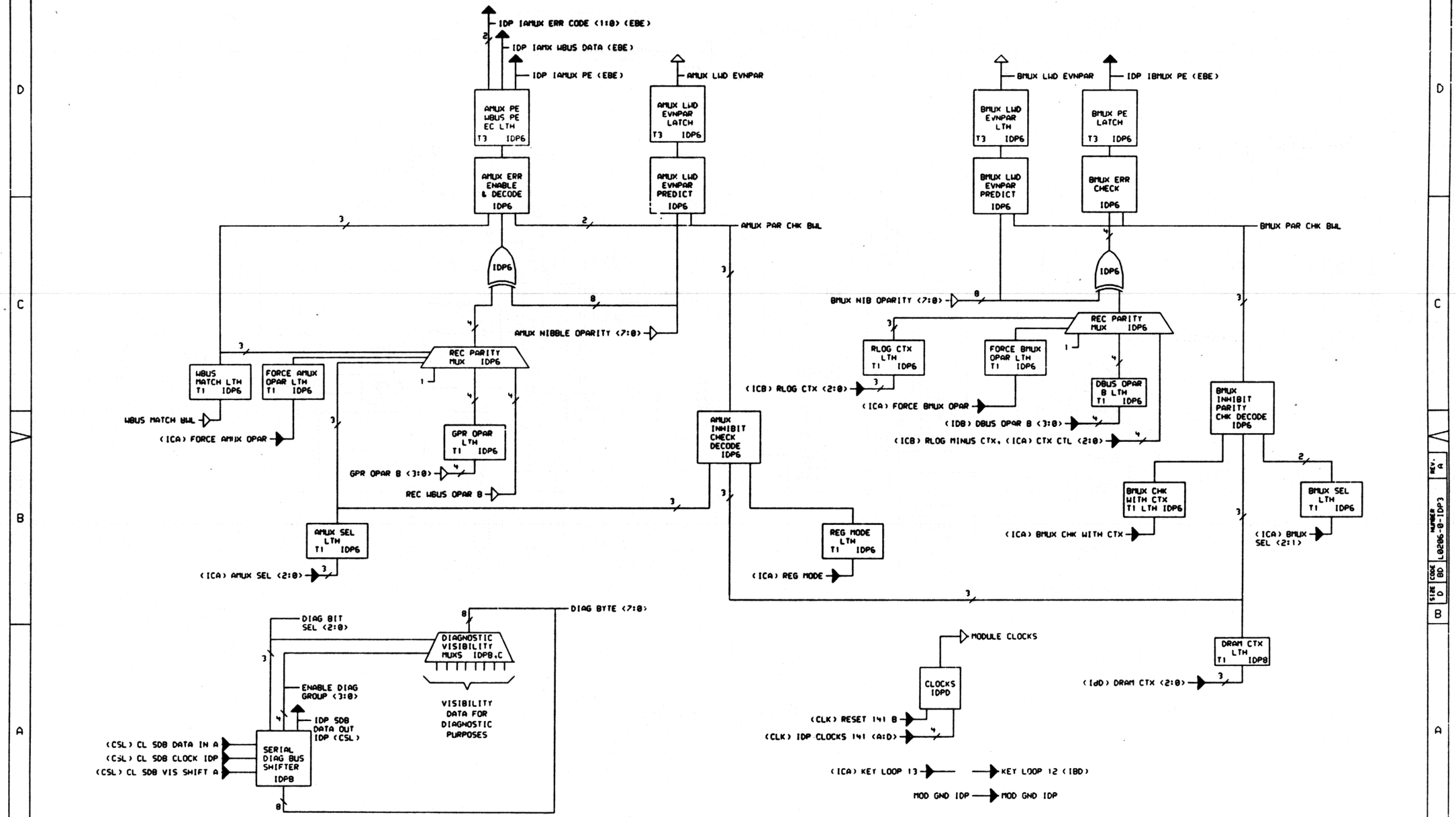
digital

DRN. ROGER G. DAME — DATE 22-OCT-84
CHK D. L. METZGER — DATE 22-OCT-84
ENG. D. BISSON — DATE 22-OCT-84
BOARD LOCATION:
SHEET 1 OF 1
ELF:<BOWEN>IDP2BD.DRW 28-SEP-84 07:17
FIRST USED ON OPTION/MODEL:
NEXT HIGHER ASSEMBLY: D-DD-L0206-0

TITLE: IDP MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0206-0-IDP2	A

2256



REVISIONS		
CHK	CHANGE NO.	REV

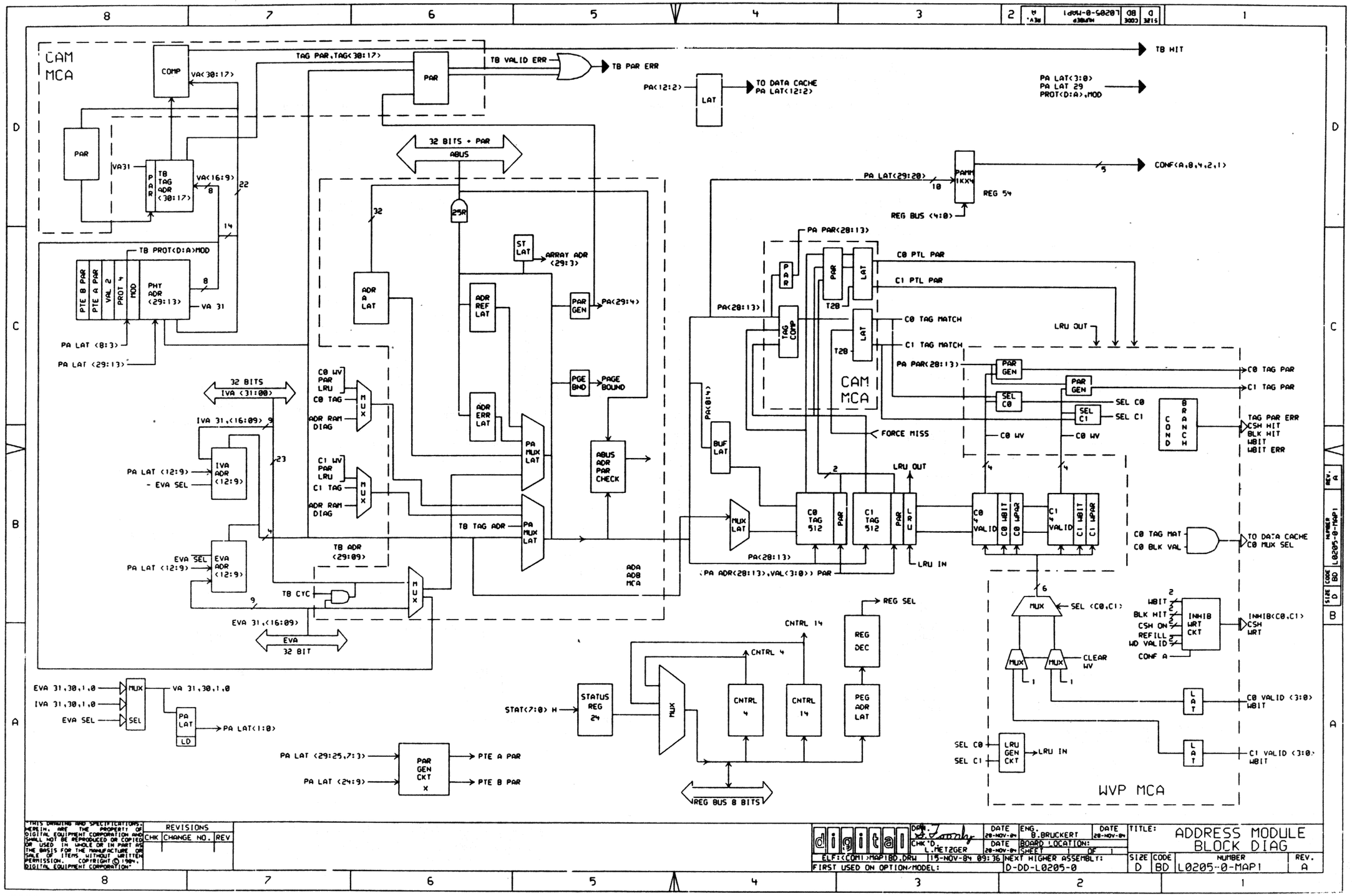
digital

DRN ROGER G. DAME 22-OCT-84 | ENG. D. BISSON 22-OCT-84
CHK L.METZGER 22-OCT-84 | BOARD LOCATION:
ELF:<BOWEN>IDP3BD.DRW 14-SEP-84 14:27 | SHEET 1 OF 1
FIRST USED ON OPTION/MODEL: | NEXT HIGHER ASSEMBLY: D-DD-L0206-0

TITLE: IDP MODULE BLOCK DIAGRAM

SIZE	CODE	NUMBER	REV.
D	BD	L0206-0-IDP3	A

225



REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN J.Landy 28-NOV-84 | ENG. B.BRUCKERT 28-NOV-84 | TITLE: ADDRESS MODULE BLOCK DIAG

CHK D. L.METZGER 28-NOV-84 | BOARD LOCATION: SHEET 1 OF 1

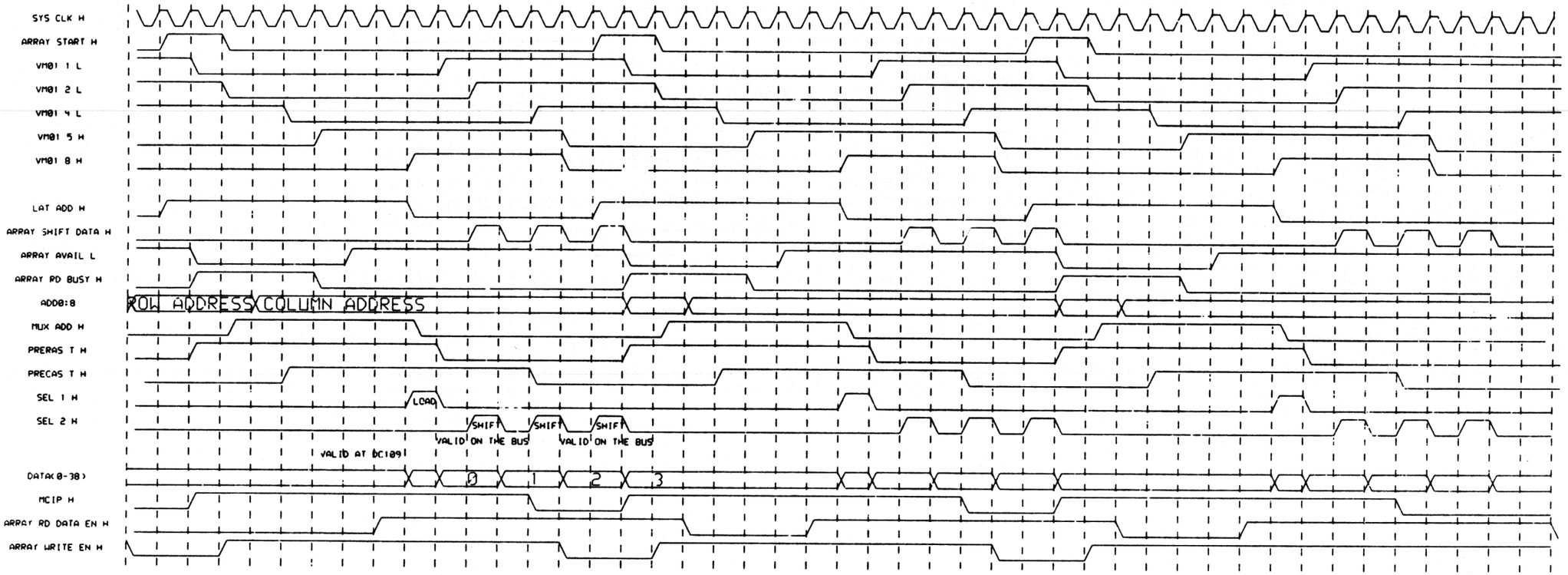
ELF:<COMI>MAP1BD.DRW 15-NOV-84 09:36 | NEXT HIGHER ASSEMBLY: D-DD-L0205-0

FIRST USED ON OPTION/MODEL:

SIZE	CODE	NUMBER	REV.
D	BD	L0205-0-MAP1	A

2258

ARRAY TIMING READ CYCLE



SHEET 1 OF 1

REVISIONS		
CHK	CHANGE NO.	REV

digital

DRN. D.Cromby 02-APR-84 08:17 | CHK D. | DATE 06-SEP-84 | ENG. | DATE 06-SEP-84 | BOARD LOCATION: | SHEET 1 OF 1

ELF:<BOWEN>VTIMED.DRW

FIRST USED ON OPTION/MODEL: MS66-BA

NEXT HIGHER ASSEMBLY: D-DD-L0200-BA

TITLE: 4 MBYTE READ CYCLE

SIZE	CODE	NUMBER	REV.
D	TD	L0200-BA-VTII	B00

2259

2 AND 4 WORD WRITE CYCLES

SYS CLK H

(B49) MCC8 ARRAY START H

VM01 LATADD H

VM01 1 L

VM01 2 L

VM01 4 L

VM01 5 H

VM01 8 H

(B69) MCC8 ARRAY SHIFT DATA H

(B37) ARRAY AVAIL H

VM01 MUXADD E H

ADDRESSES — ROW ADDR | COL ADDR | ROW ADDR | COL ADDR

VALID @ PINS

VALID @ RAMS

(B5) ARRAY WRT ENA H

(B6) MCC8 ARRAY 4WD WRT H

(B7) ARRAY ADR 03 H

VM01 MEMORY CYCLE IN PROGRESS H

VM01 PRERAS T H

VM01 PPECAS T H

VM04 WRITE WORD XX L (@ RAMS)

VM02 DC109 SEL1 X H

VM02 DC109 SEL2 X H

TTLEN (@ DC109)

DATA WORD — 0 | 1 | 0 | 1 | 2 | 3

SHEET 1 OF 1

REVISIONS		
CHK	CHANGE NO.	REV

digital

DSN: L. Kendall — DATE 06-SEP-84
CHK: D. — DATE

ENG. — DATE 06-SEP-84

BOARD LOCATION:
SHEET 1 OF 1

ELF:<BOWEN.WRTTIM.DFW 02-APR-84 08:17
FIRST USED ON OPTION/MODEL: MS86-BA

NEXT HIGHER ASSEMBLY: D-DD-L0200-BA

TITLE: 4MBYTE 2WD WRT/4 WRT

SIZE	CODE	NUMBER	REV.
D	TD	L0200-BA-WRT1	B00

2260