

Digital Semiconductor 21172 Core Logic Chipset

Product Brief

March 1996



Description

The Digital Semiconductor 21172 core logic chipset provides the quickest, most cost-effective Alpha solution for system providers in the high-performance PC market. The chipset gives the system designer flexibility in building the memory and I/O subsystem, and requires minimal discrete logic on the module. The chipset includes an interface to a 64-bit or 32-bit PCI local bus and control and data paths for the Digital Semiconductor 21164 Alpha microprocessor, memory, and optional external L3 backup cache.

The chipset uses two unique gate arrays:

- Digital Semiconductor 21172-BA (DSW—data switch) in a 208-pin plastic quad flat pack (PQFP) package
- Digital Semiconductor 21172-CA (CIA—control, I/O interface, and address) in a 388-pin plastic ball grid array (PBGA) package

Features

The Digital Semiconductor 21172 core logic chipset, which includes one CIA chip and four DSW chips, enables the highest performance of client systems in the computer industry. Some of its features include:

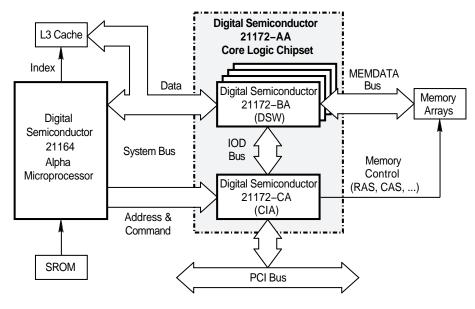
- Central processing unit
- Supports the Digital Semiconductor 21164 Alpha microprocessor running at speeds of 366, 400, or 433 MHz
- Data paths
- 64-bit, ECC-protected data path between CIA and DSW chips
- 128-bit, ECC-protected data path between 21164 and DSW
- 128-bit or 256-bit ECC-protected data path between DSW chips and memory arrays
- Timing
- Supports system clock frequencies up to 33 MHz
- PCI clock, cache, and memory clock periods are integer multiples of the 21164 clock period

Memory

- Supports up to 8GB of physical memory with ECC protection
- Supports industry-standard 36-bit single inline memory modules (SIMMs) at speeds of 70 ns or faster in standard DRAM configurations
- High-performance PCI
- Compliant with PCI Local Bus Specification, Revision 2.0
- 64-bit or 32-bit, 33-MHz multiplexed address and data
- Scatter-gather map support
- No glue logic required to connect PCI-compliant devices
- Optional L3 backup cache
- Third-level cache for microprocessor
- Cache size from 1MB to 16MB
- 64-byte block size
- Write-back, ECC-protected



Digital Semiconductor 21172-AA Core Logic Chipset System Block Diagram



Digital Semiconductor 21172 Core Logic Chipset Characteristics Characteristic **Specification** Vss 0.0 V Power supply Vdd 3.3 V ±5% Operating temperature $Tamax=40^{\circ}C (104^{\circ}F)$ -55° C to 125° C (-67° F to 257° F) Storage temperature range Power dissipation @ Vdd = 3.3 V and 2.0 W maximum (CIA chip) Frequency = 33 MHz1.5 W maximum (DSW chip) 388-pin plastic ball grid array **Packaging** (PBGA) (CIA chip) 208-pin plastic quad flat pack

(PQFP) (DSW chip)

The following components can be used to build a high-performance PC:

- Digital Semiconductor 21164 Alpha microprocessor running at speeds of 366, 400, or 433 MHz
- Digital Semiconductor 21172 core logic chipset
- •L3 Bcache array (optional)
- Main-memory array
- Serial ROM (for CPU initial load)
- CPU clock and phase-locked loop (PLL) for system clocks
- Industry-standard support logic:
- PCI arbiter
- Reset logic
- Flash ROM (for PALcode and initialization instructions)
- PCI and ISA peripheral devices
- Enclosure and power supply

For More Information

To learn more about the availability of the Digital Semiconductor 21172 Core Logic Chipset, contact your local semiconductor distributor. To learn more about Digital Semiconductor's product portfolio, contact the Digital Semiconductor Information Line:

1-800-332-2717

Outside North America, call:

+1-508-628-4760

While Digital believes the information in this publication is correct as of the date of publication, it is subject to change without notice.

© Digital Equipment Corporation 1996.

All rights reserved Printed in U.S.A.

EC-QUQHA-TE

Digital, Digital Semiconductor, and the DIGITAL logo are trademarks of Digital Equipment Corporation. Digital Semiconductor is a Digital Equipment Corporation business.

All other trademarks and registered trademarks are the property of their respective owners.